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HSF Property:ROHS

ACER

BAP41/BAP51/BAP52/BXP41/SJM52
UMA+Discrete(SW Gfx)
MAIN BOARD

2009.06.30

Tuesday, June 30, 2009		A02
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXXX

INVENTEC

TITLE BAP41/BAP51 (Montevina SFF)

SIZE	CODE	DOC.NUMBER	REV
C	A02	D-CS-1310A292001-ALG	A02

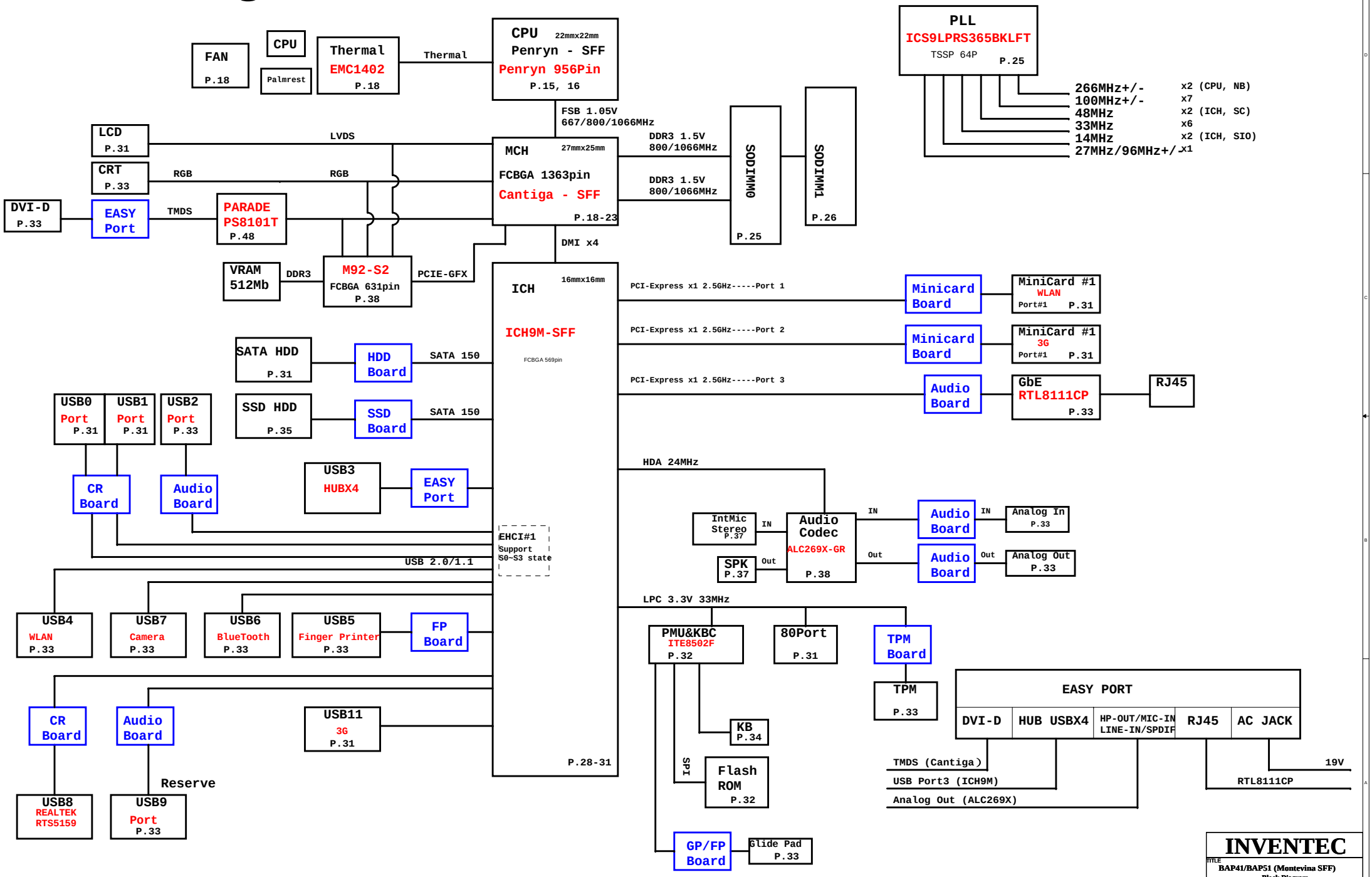
SHEET 1 of 49

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title
2. Schematic Page DESCR
3. Block Diagram
4. Annotations
5. Schematic Modify
6. Timing Diagram
7. Power Block Diagram
8. Adaptor in/Charge
9. 5VLA/5VA/3VA
10. 3VS/5VS/1.5V (DDR3)
11. 1.05VS/1.5S/1.8V/1.5VA
12. Power Latch/1.5VS/SCREW HOLE
13. CPU Core Power
14. GPU Core Power
15. Penryn Processor(1/2)
16. Penryn Processor(2/2)
17. CPU Thermal
18. Cantiga Host(1/6)
19. Cantiga DMI/Graph(2/6)
20. Cantiga DDRIII(3/6)
21. Cantiga Power(4/6)
22. Cantiga Power(5/6)
23. Cantiga Ground(6/6)
24. Clock Generator
25. DDR3 SDRAM SO-DIMM0
26. DDR3 SDRAM SO-DIMM1
27. ICH9M CPU/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD/CRT
32. KBC ITE8502E-L
33. IO CN
34. IO CN
35. IO CN
36. Audio Codec
37. EASY PORT CN/ LEVEL SHIFTER
38. M92-S2(1/5)
39. M92-S2(2/5)
40. M92-S2(3/5)
41. M92-S2(4/5)
42. M92-S2(5/5)
43. DDR3 VRAM
44. HyBrid Switch
45. dGPU Power
46. dGPU Power
47. dGPU Power
48. HDD Board
49. TPM Board

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:	3.0V~3.3V~3.6V	
	Super I/O: IT8305E		
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

INVENTEC

TITLE BAP41/BAP51 (Montevina SFF)
ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Monday, June 29, 2009 SHEET 4 of 49

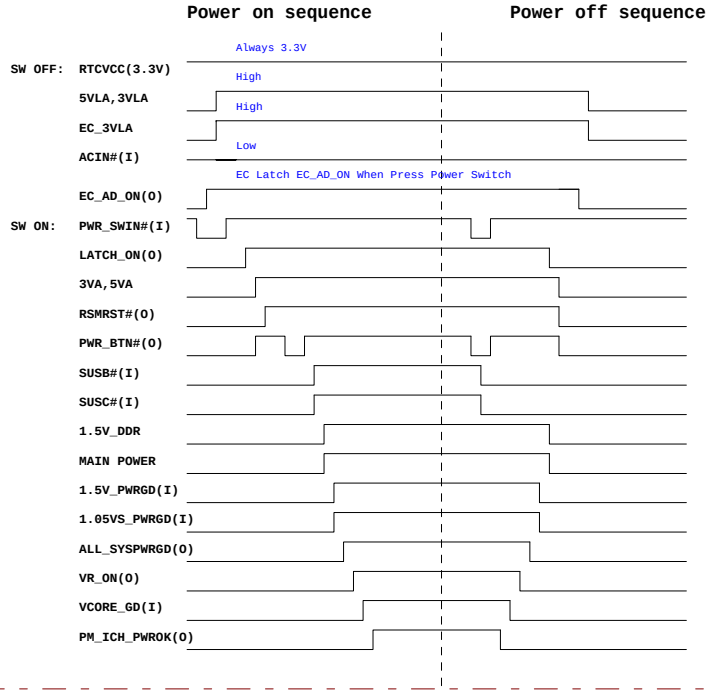
6.Schematic modify Item and History :

INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) Schematic Modify			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
CHANGE by Shiun-Chin Chang	DATE Monday, June 29, 2009	SHEET 5 of 49	

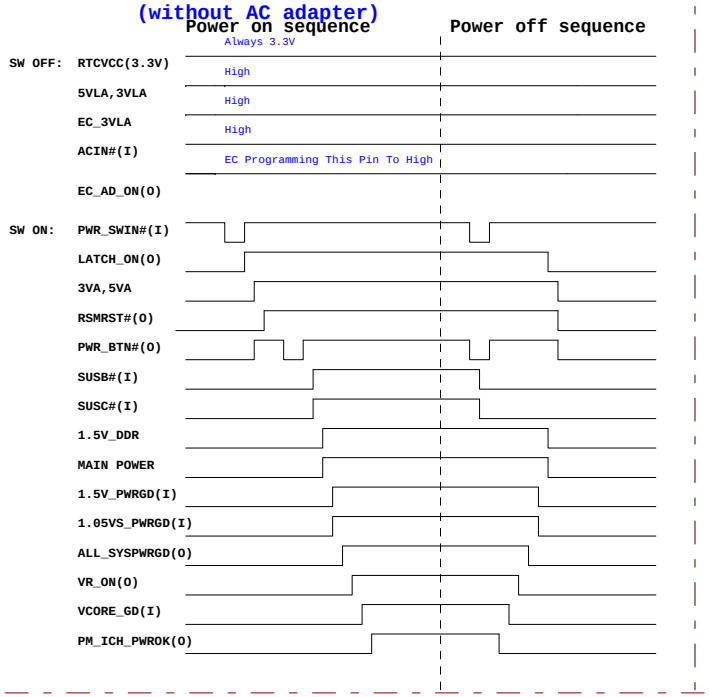
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

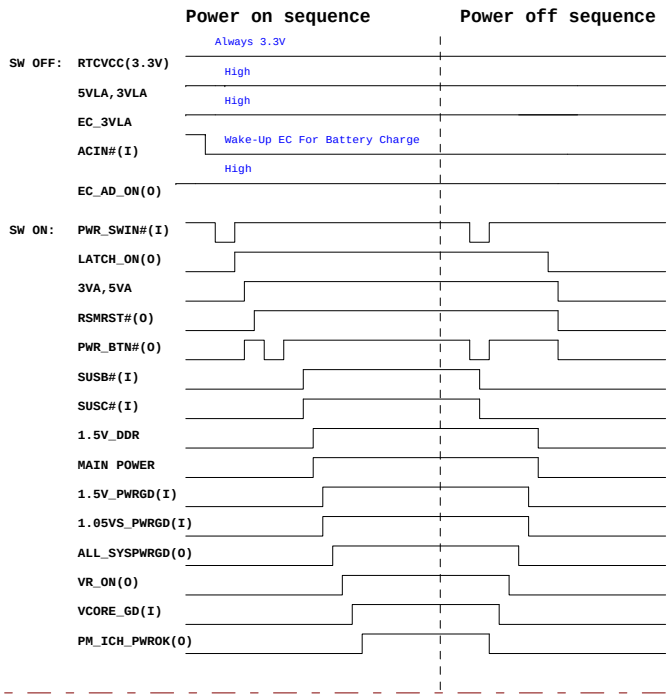
Power on/off sequence AC insert (without Battery Pack)



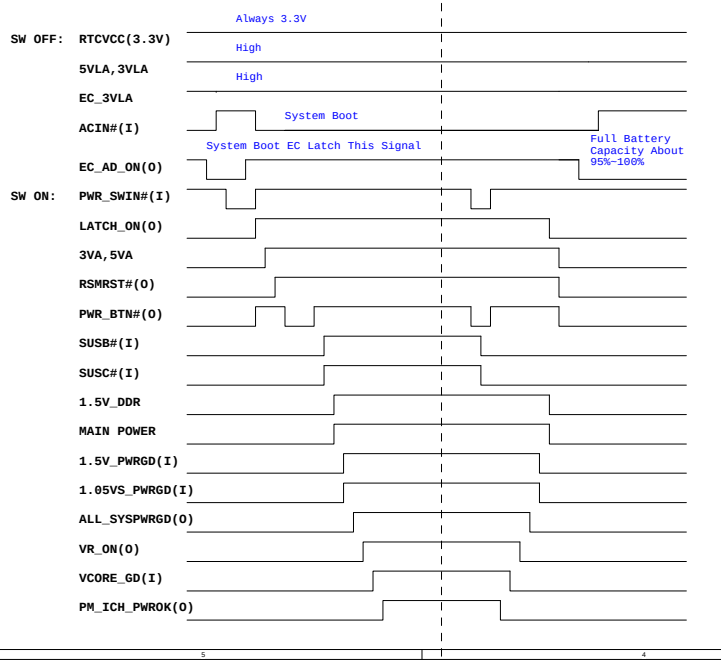
Power on/off sequence Battery insert (without AC adapter)



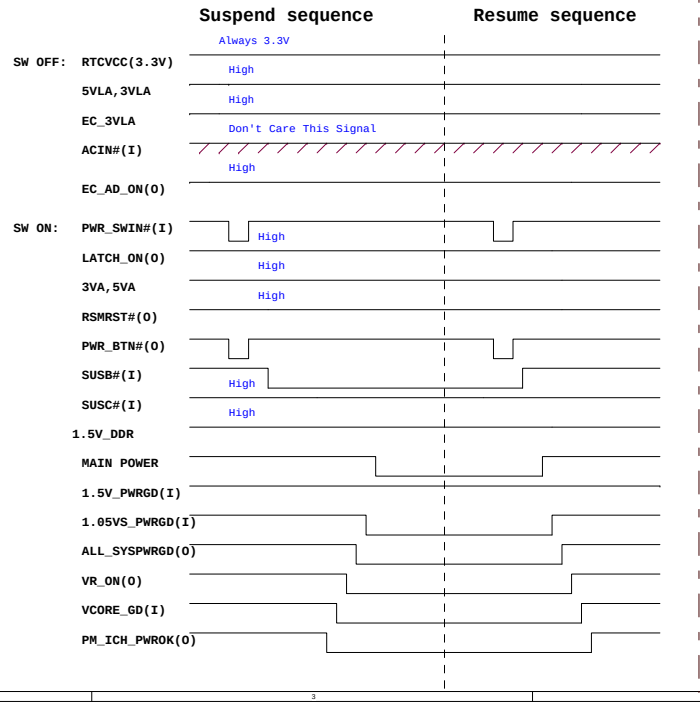
Power on/off sequence AC insert(with charge over 95%)



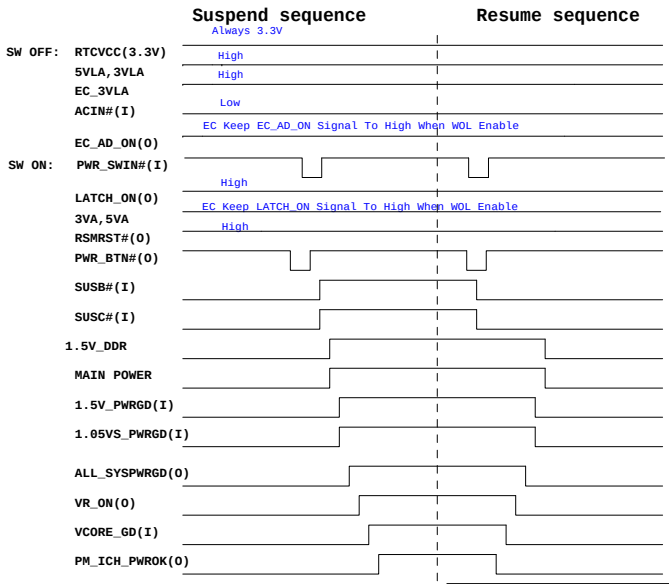
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)

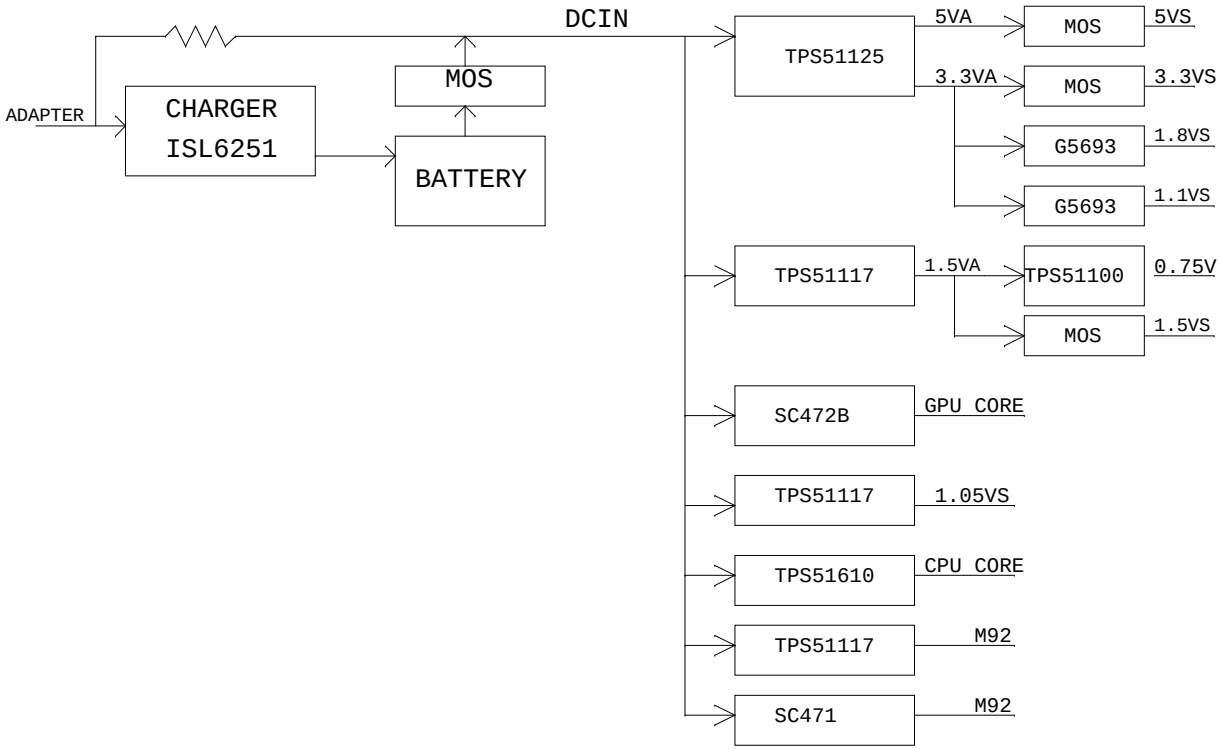


Power on/off sequence after windows shoutdown (WOL enable)



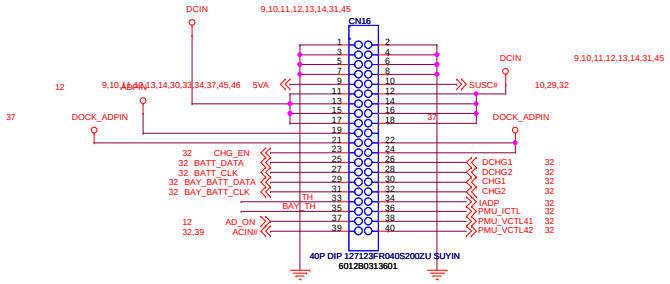
INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) Time Diagram			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Monday, June 29, 2009	SHEET 6 of 49	

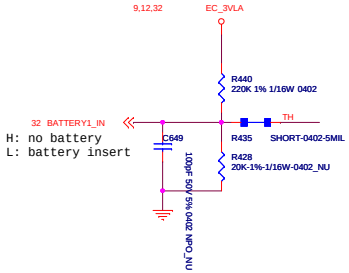
Power Block Diagram :

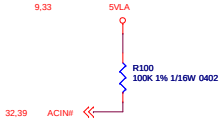


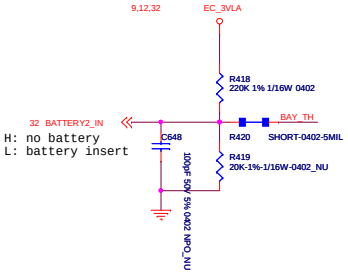
INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) Power Block Diagram			
SIZE C	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
CHANGE by Shiun-Chin Chang DATE Monday, June 29, 2009		SHEET 7 of 49	

Charger CN TO USIM/B

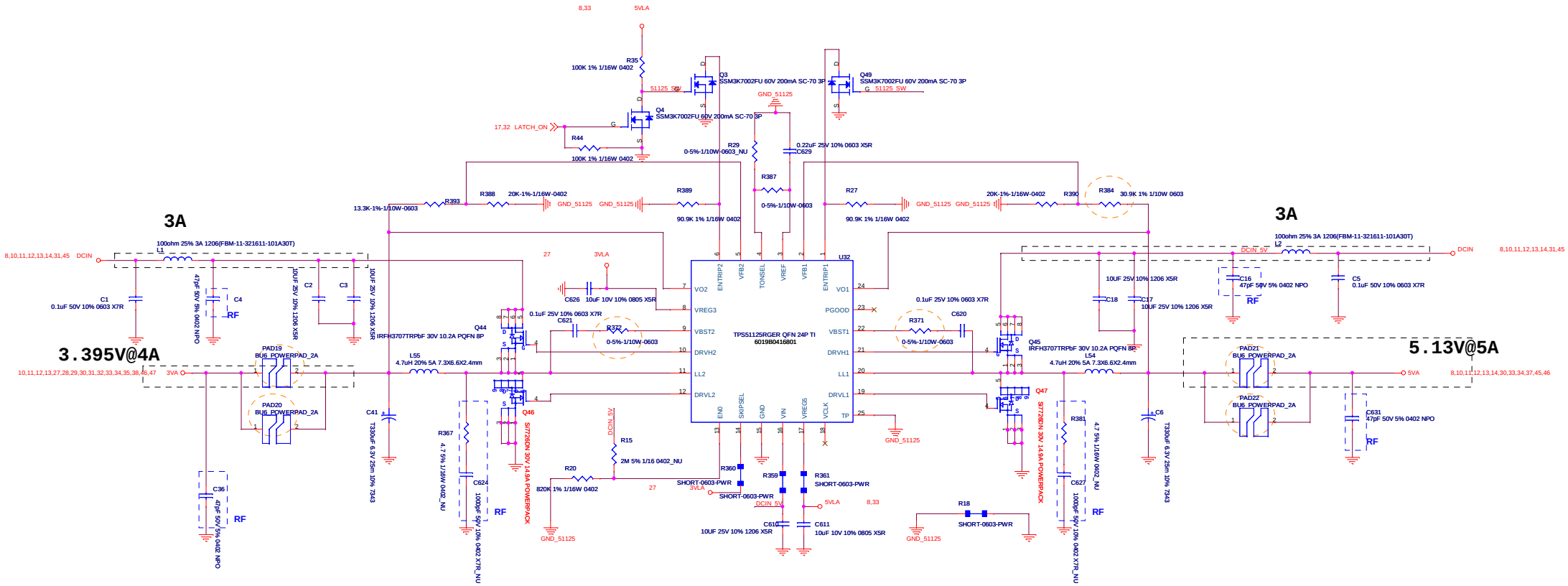




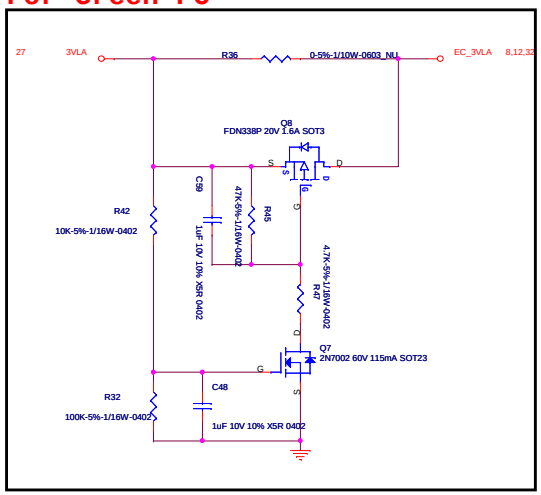




INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) Adaptor in / Charge			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A229201-ALG	REV A02
CHANGE by Shiun-Chin Chang	DATE Wednesday, July 01, 2009	SHEET 8 of 49	



For Green PC



CHANGE by	Shiun-Chin Chang	DATE	Wednesday, July 01, 2009

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF) 5VLA/5VA/3VLA/3VA

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A229201-ALG	A02

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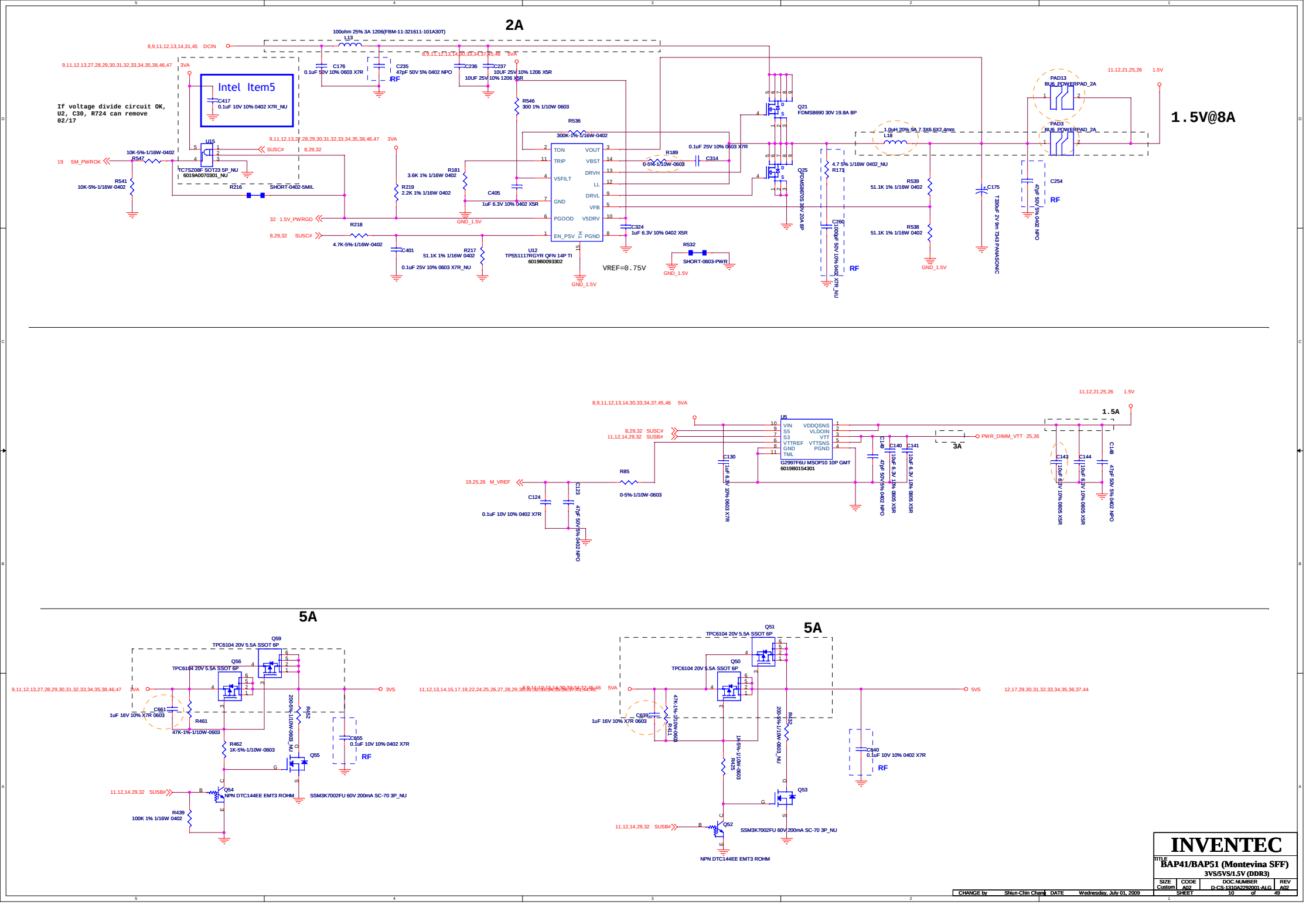
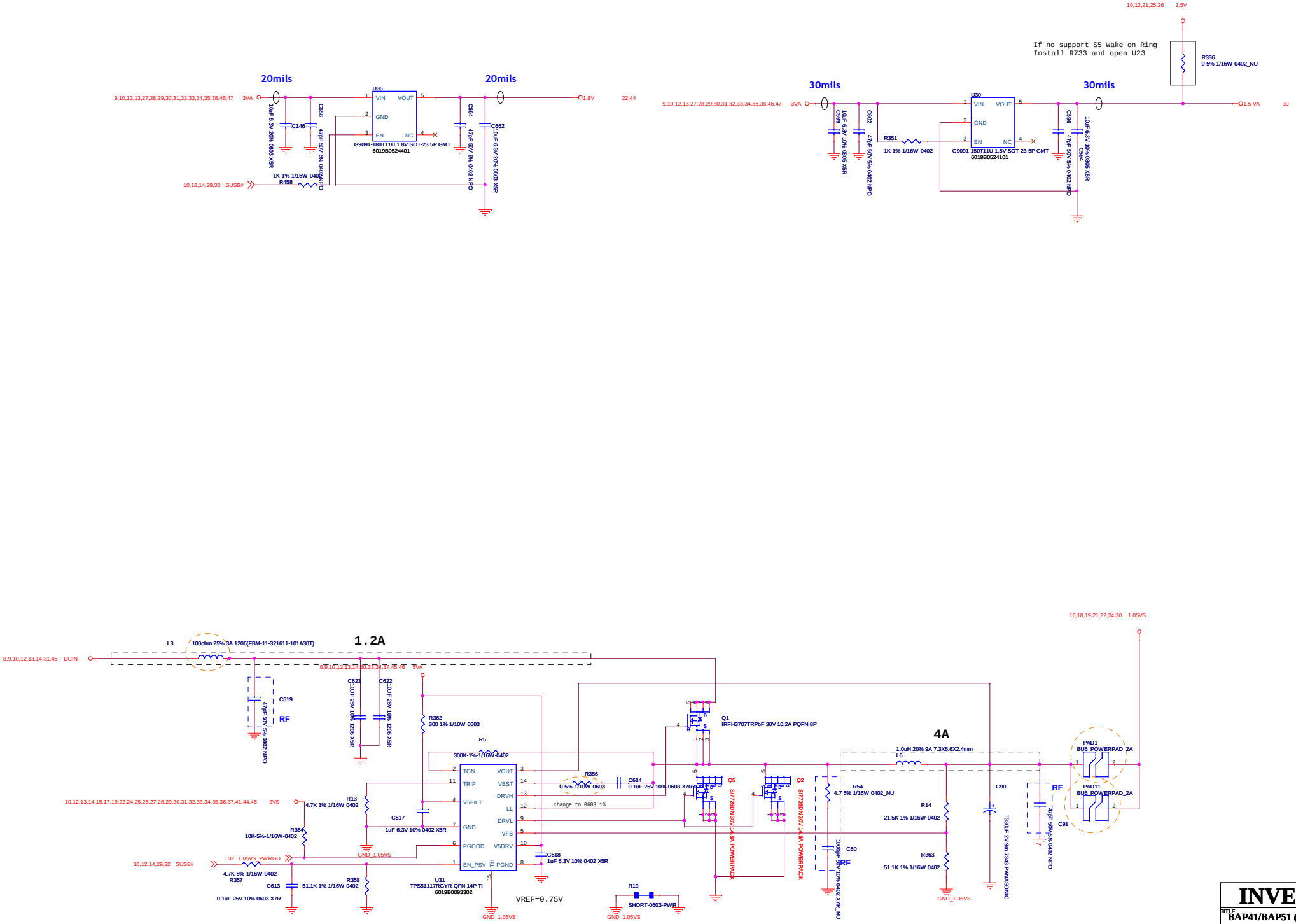


INVENTEC

TITLE BAP41/BAP51 (Montevina SFF)
3VS/5VS/1.5V (DDR3)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009 SHEET 10 of 49


20mils
20mils
30mils
30mils
If no support S5 Wake on Ring
Install R733 and open U23
U36
G9091-180T11U 1.8V SOT-23 5P GMT
6019B0524401
U30
G9091-150T11U 1.5V SOT-23 5P GMT
6019B0524101
R336
0-5%-1/16W-0402_NU
1.5V
1.8V
1.5 VA
3VA
SUSB#
R458
1K-1%-1/16W-0402
R351
1K-1%-1/16W-0402
1.2A
4A
L3
100ohm 25% 3A 1206(FBM-11-321611-101A30T)
DCIN
5VA
3VS
1.05VS
Q1
IRFH3707TRPbF 30V 10.2A PQFN 8P
Q5
SI7726DN 30V 14.9A POWERPACK
Q2
SI7726DN 30V 14.9A POWERPACK
L6
1.0uH 20% 9A 7.3X6.6X2.4mm
R5
300K-1%-1/16W-0402
R362
300 1% 1/10W 0603
R356
0-5%-1/10W-0603
C614
0.1uF 25V 10% 0603 X7R
change to 0603 1%
R54
4.7 5% 1/16W 0402_NU
R14
21.5K 1% 1/16W 0402
R363
51.1K 1% 1/16W 0402
C90
T330uF 2V 9m 7343 PANASONIC
C91
47pF 50V 5% 0402 NPO
PAD1
BU6_POWERPAD_2A
PAD11
BU6_POWERPAD_2A
C60
7000pF 50V 10% 0402 X7R_NU
C619
47pF 50V 5% 0402 NPO
C623
10uF 25V 10% 1206 X5R
C622
10uF 25V 10% 1206 X5R
R13
4.7K 1% 1/16W 0402
R364
10K-5%-1/16W-0402
C617
1uF 6.3V 10% 0402 X5R
C618
1uF 6.3V 10% 0402 X5R
R357
4.7K-5%-1/16W-0402
C613
0.1uF 25V 10% 0603 X7R
R358
51.1K 1% 1/16W 0402
U31
TPS51117RGYR QFN 14P TI
6019B0093302
TON
TRIP
V5FILT
GND
PGOOD
EN_PSV
VOUT
VBST
DRVH
LL
DRVL
VFB
V5DRV
PGND
VREF=0.75V
R19
SHORT-0603-PWR
GND_1.05VS
RF
INVENTEC
TITLE
BAP41/BAP51 (Montevina SFF)
1.05VS/1.5S/1.8V/1.5VA
SIZE Custom
CODE A02
DOC.NUMBER D-CS-1310A2292001-ALG
REV A02
CHANGE by Shiun-Chin Chang
DATE Wednesday, July 01, 2009
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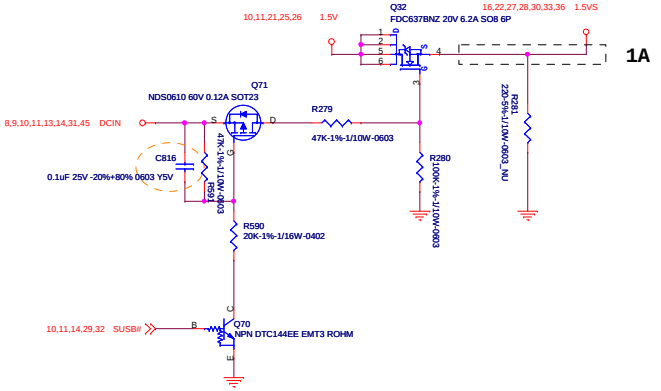
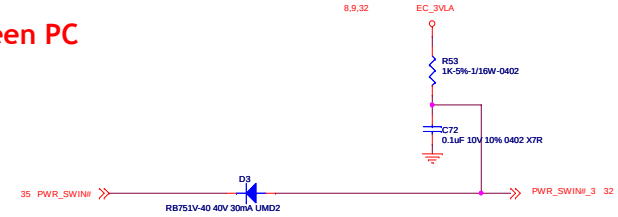
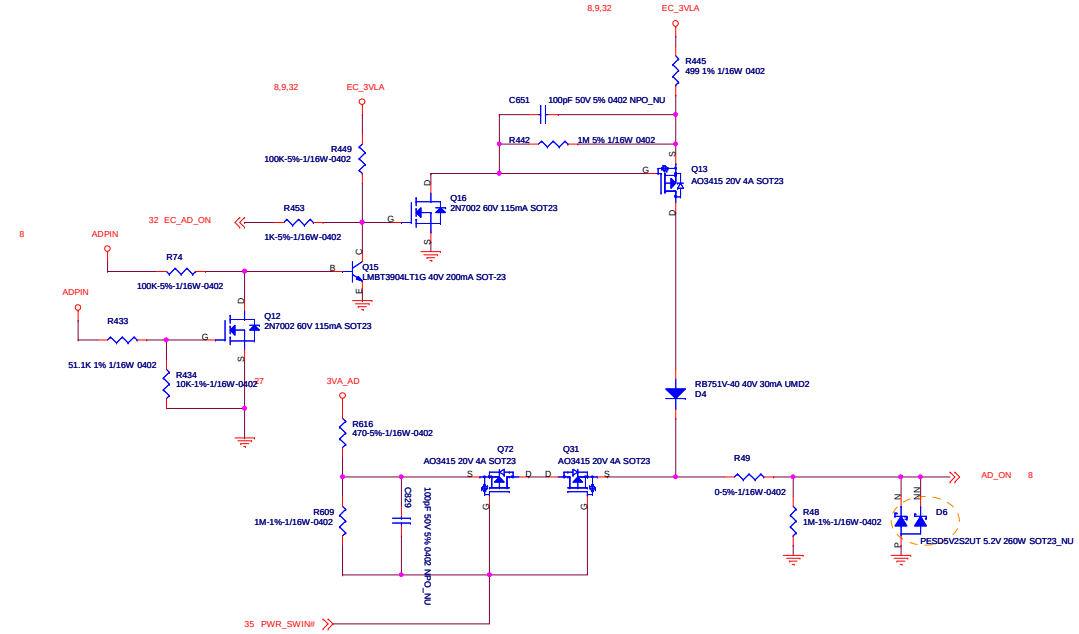
1.5VS



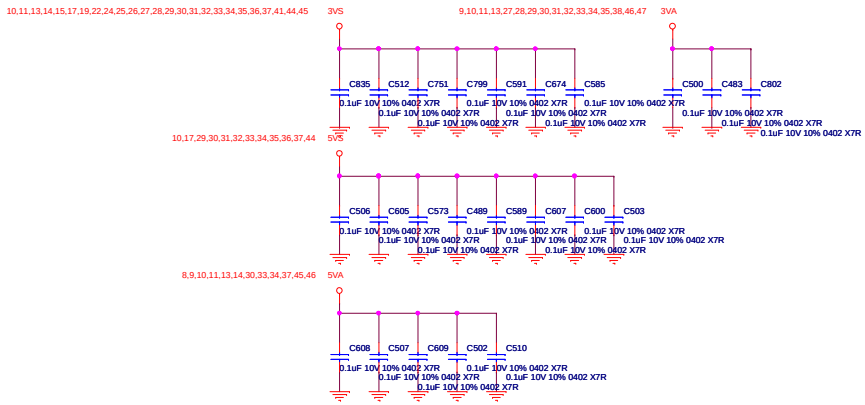
For Green PC

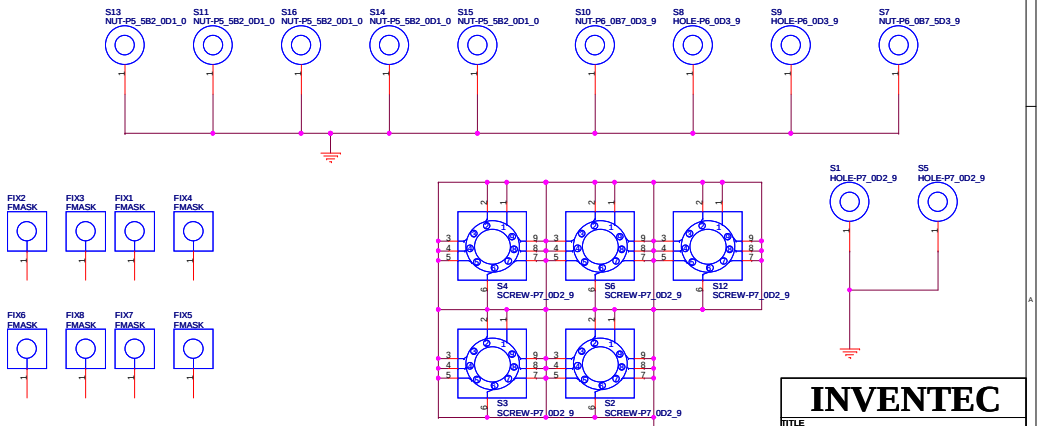


None Green PC ---- NU

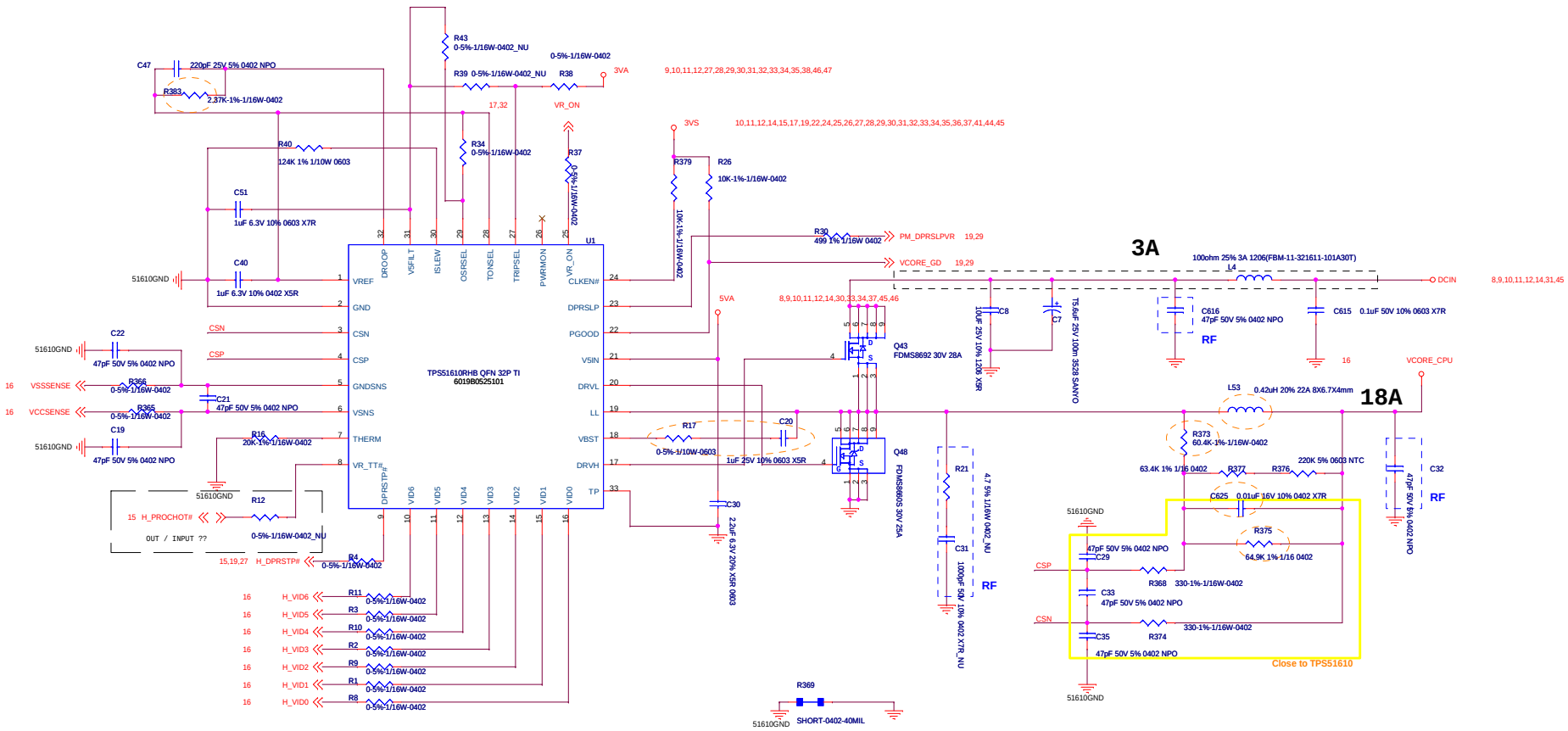


EMI Cap





INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) Power on latch			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A229001-ALG	REV A02
CHANGE by Shiun-Chin Chang	DATE Wednesday, July 01, 2009	SHEET 12 of 49	

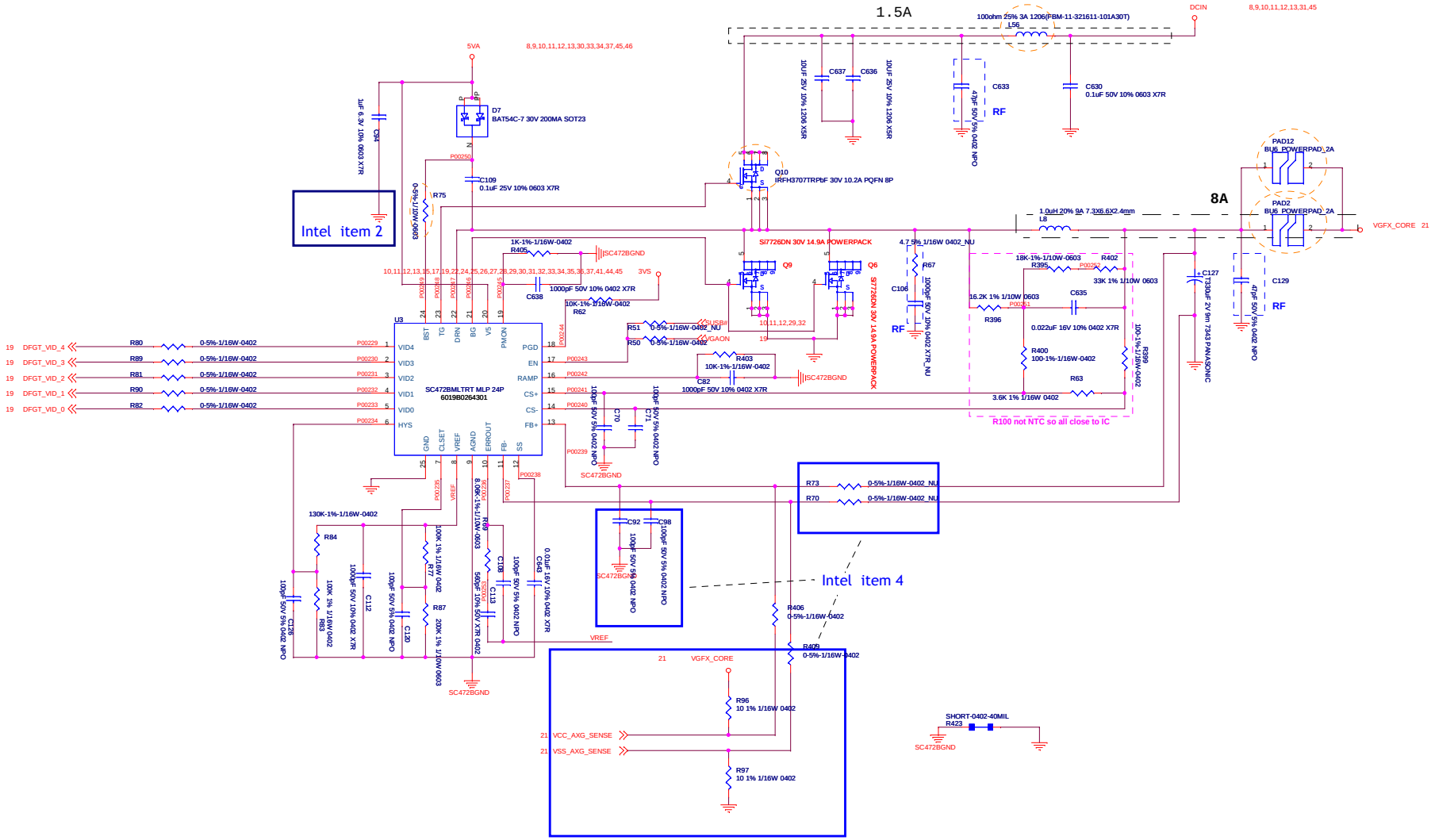


INVENTEC

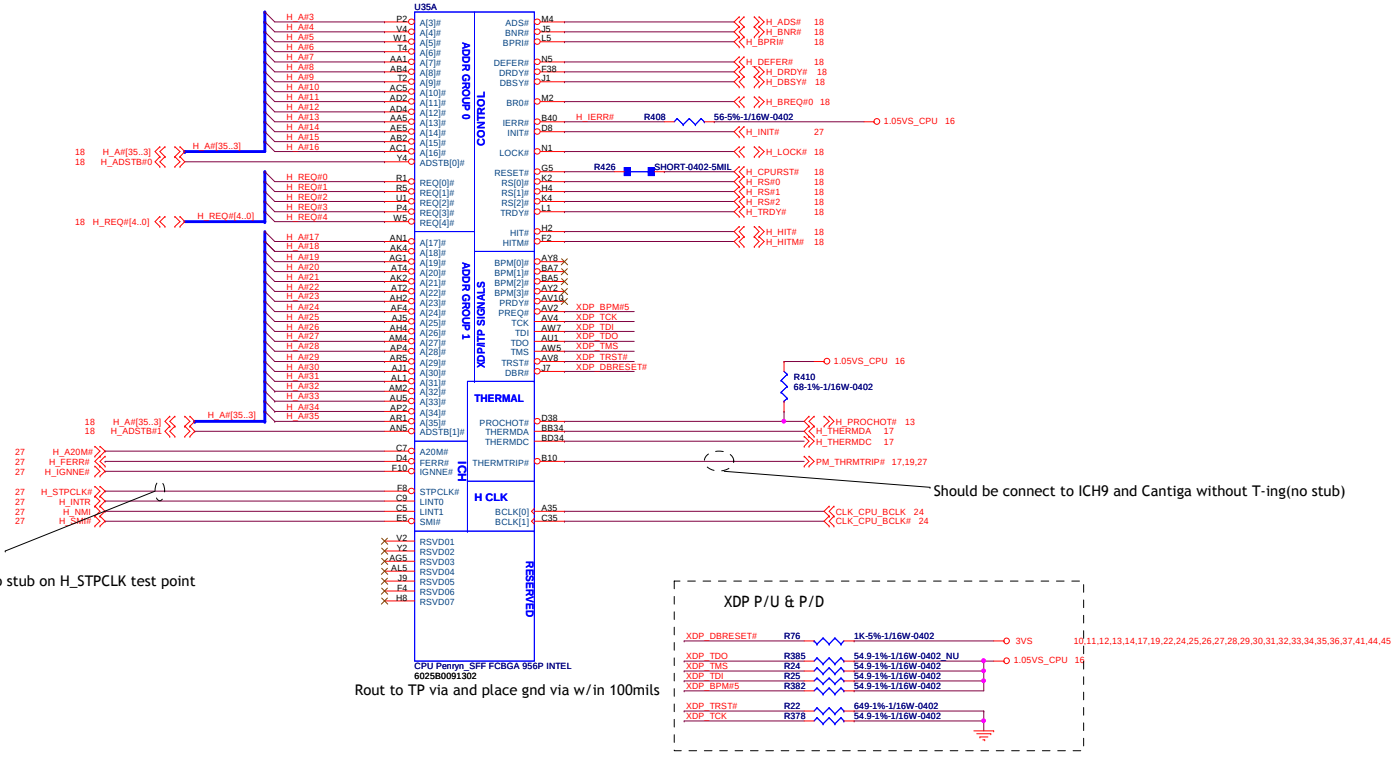
TITLE
BAP41/BAP51 (Montevina SFF)
CPU Core Power

SIZE	CODE	DOC NUMBER	REV
C	A02	D-CS-1310A2292001-ALG	A02

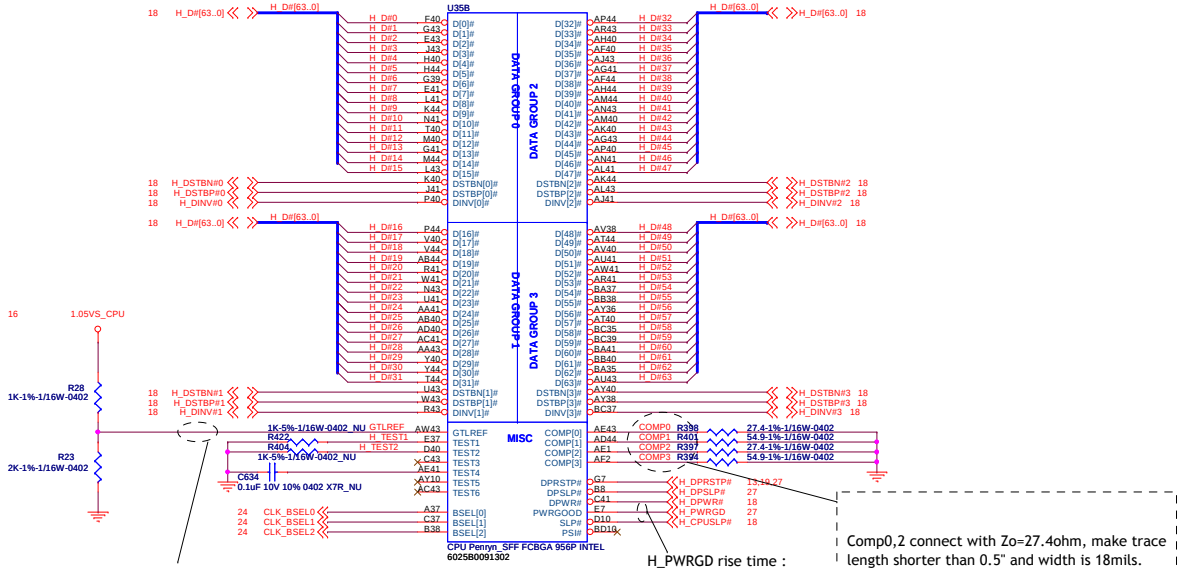
CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009 SHEET 13 of 49

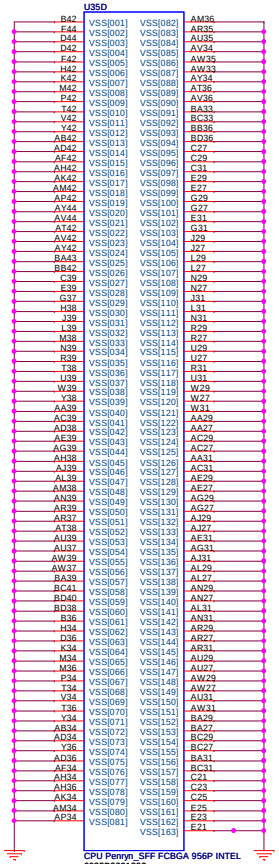


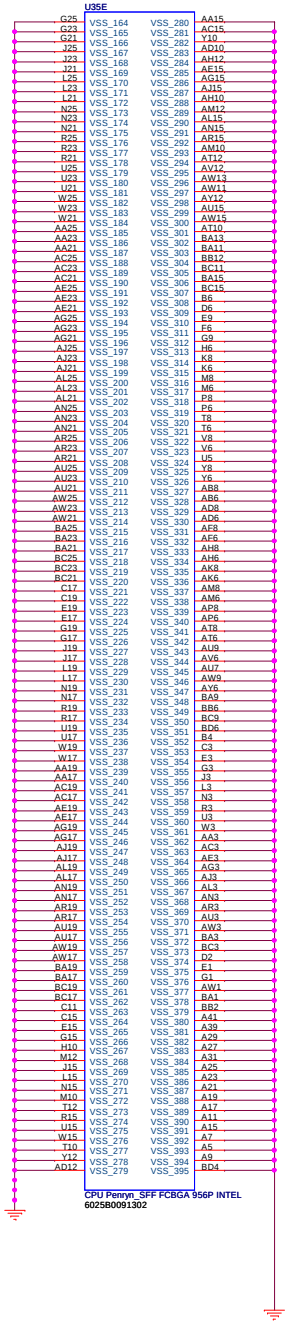
INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) GPU CORE			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A229201-ALG	REV A02
CHANGE by Shiun-Chin Chang	DATE Wednesday, July 01, 2009	SHEET 14 of 49	



A#[32-39], APM#[0-1]:Leave escape routing on for future functionality





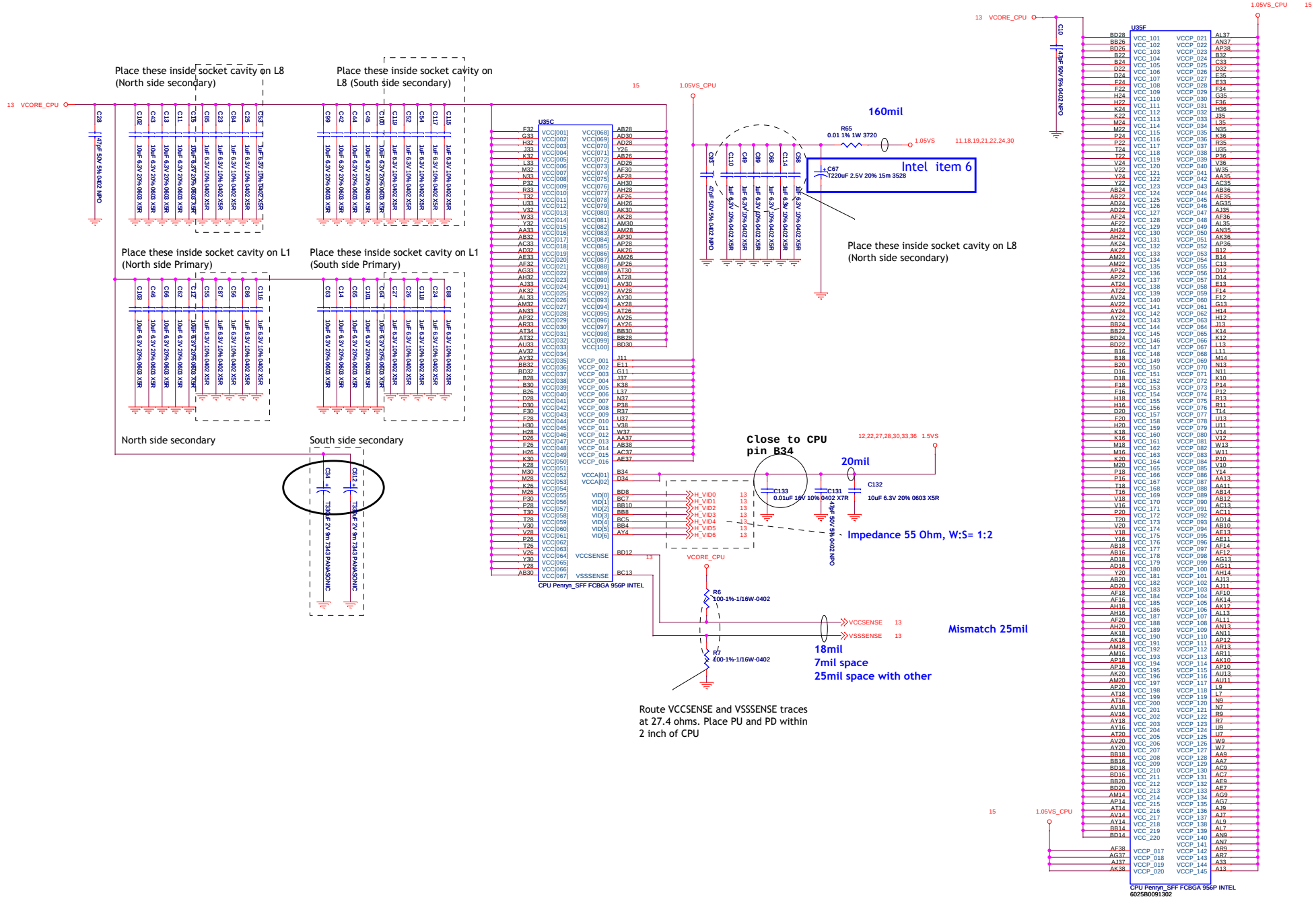


INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Penryn Processor(1/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Wednesday, July 01, 2009 SHEET 15 of 49



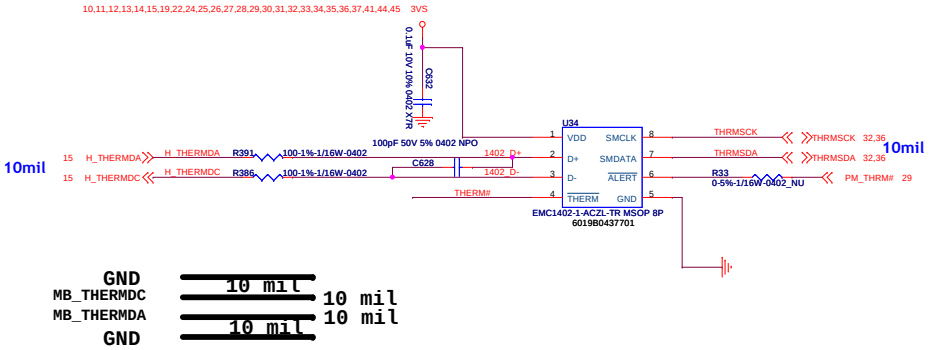
INVENTEC

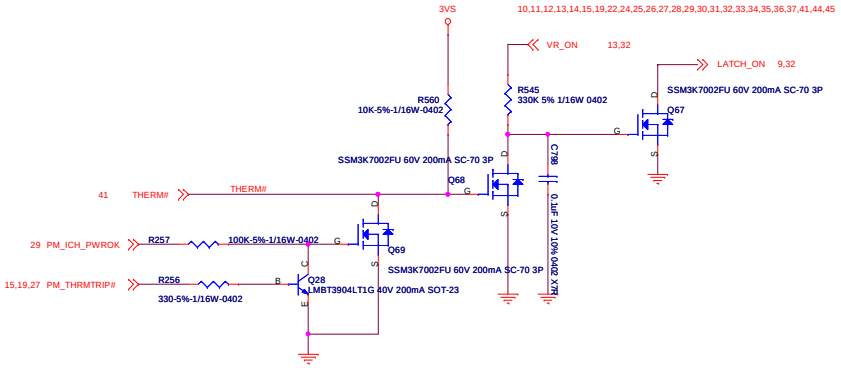
TITLE
BAP41/BAP51 (Montevina SFF)
Penryn Processor(2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

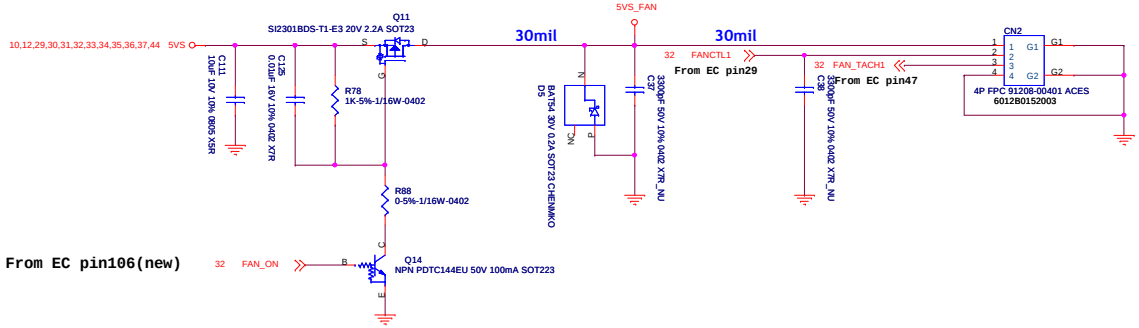
CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009 SHEET 16 of 49

THERMAL SENSOR



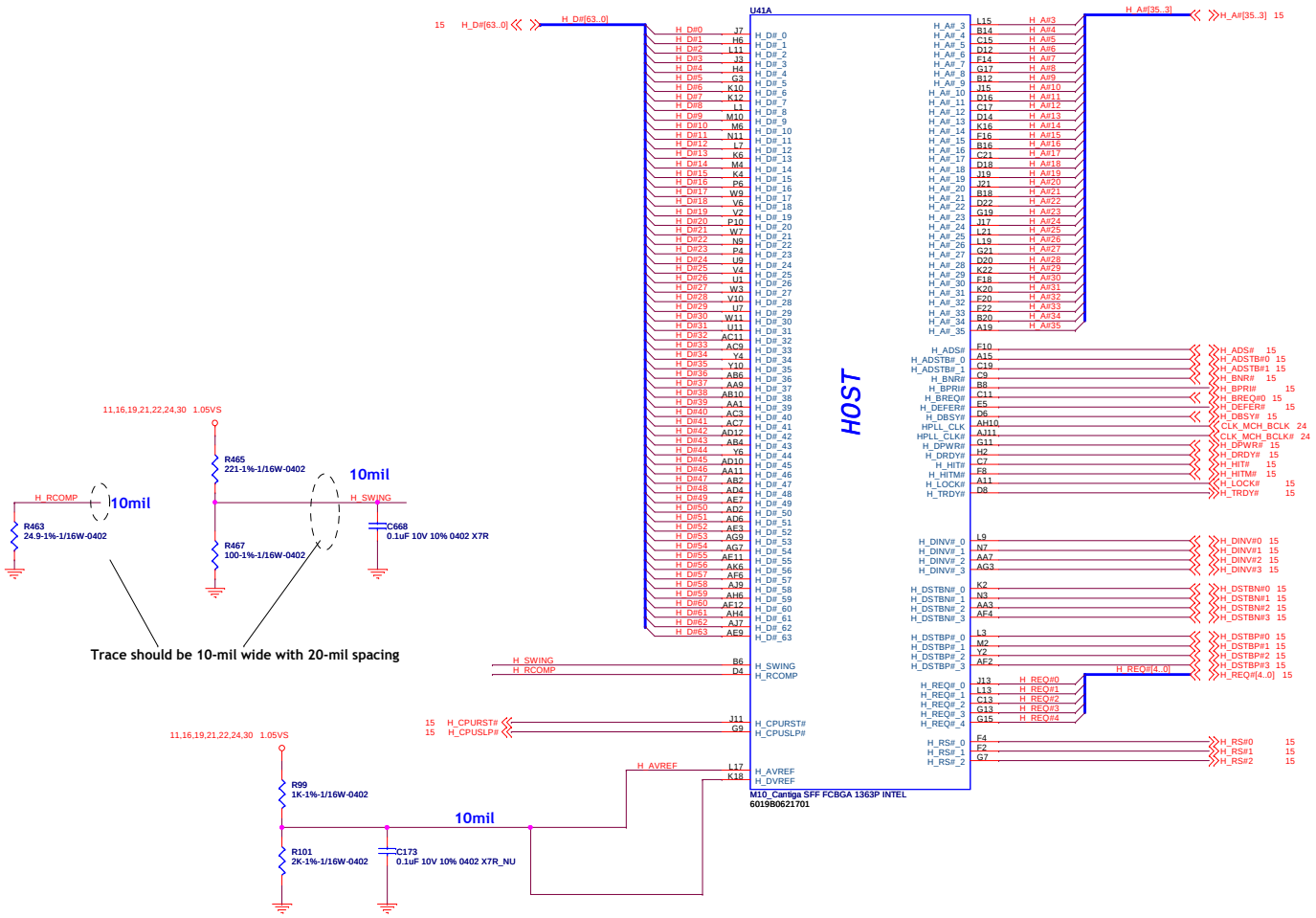


Fan control



INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) CPU Thermal			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
SHEET 17 of 49			

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009



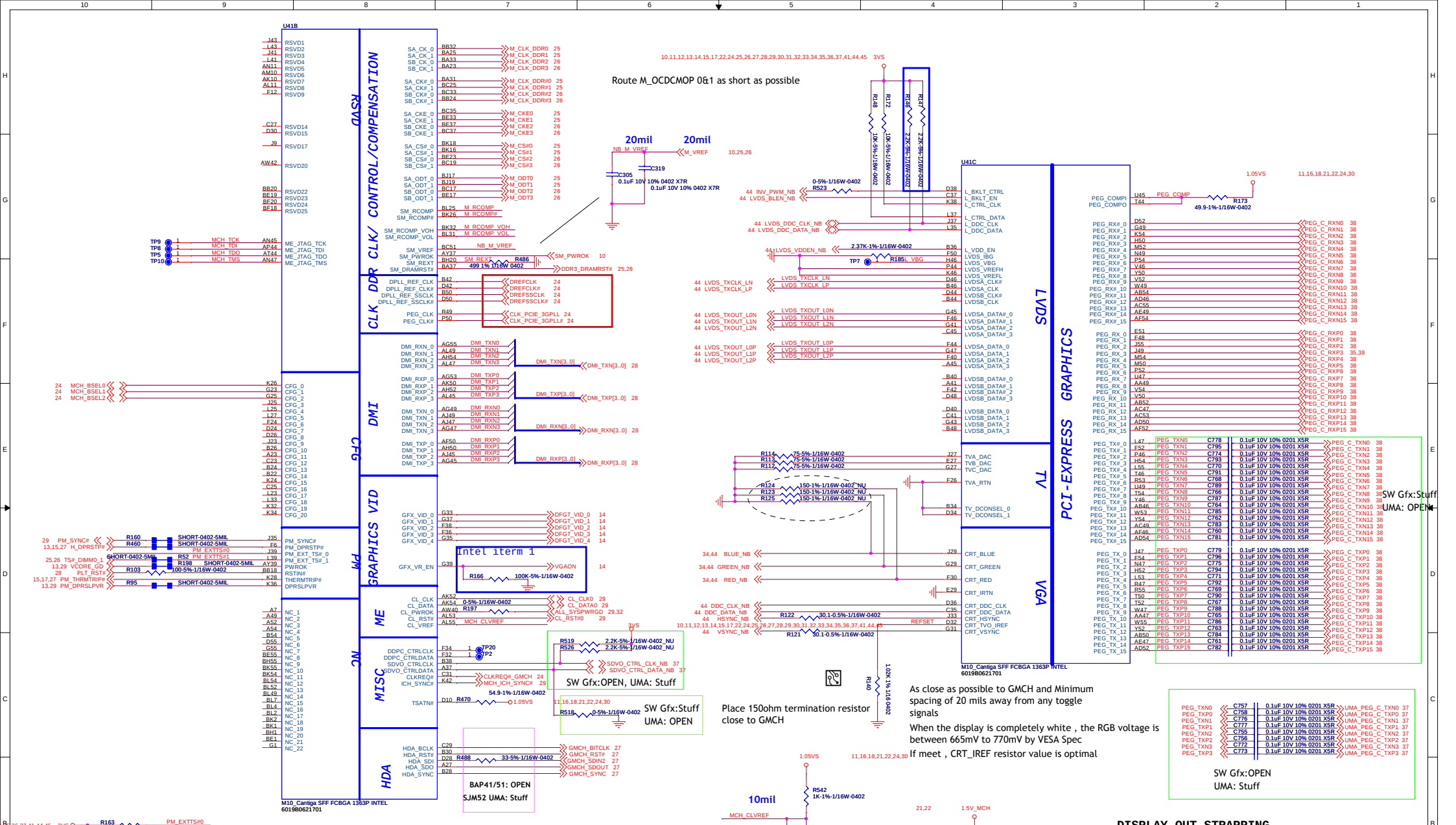
INVENTEC

TITLE
BAP41/BAP51 (Montevina SFF)
Cantiga Host(1/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A229001-ALG	A02

SHEET 18 of 49

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009



Cantiga Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only (SDVO/DP/iHDMI) or PCIE is operational	(SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port

DISPLAY OUT STRAPPING

	LOW	HIGH
SDVO_CTRLDATA	SDVO/iHDMI/DP disabled (default)	SDVO/HDMI/DP enabled
L_DDC_DATA	LFP Disabled (default)	LFP Card Present; PCIE disabled
DDPC_CTRLDATA	Digital display (iHDMI/DP) disabled (default)	Digital display (iHDMI/DP) enabled

INVENTEC

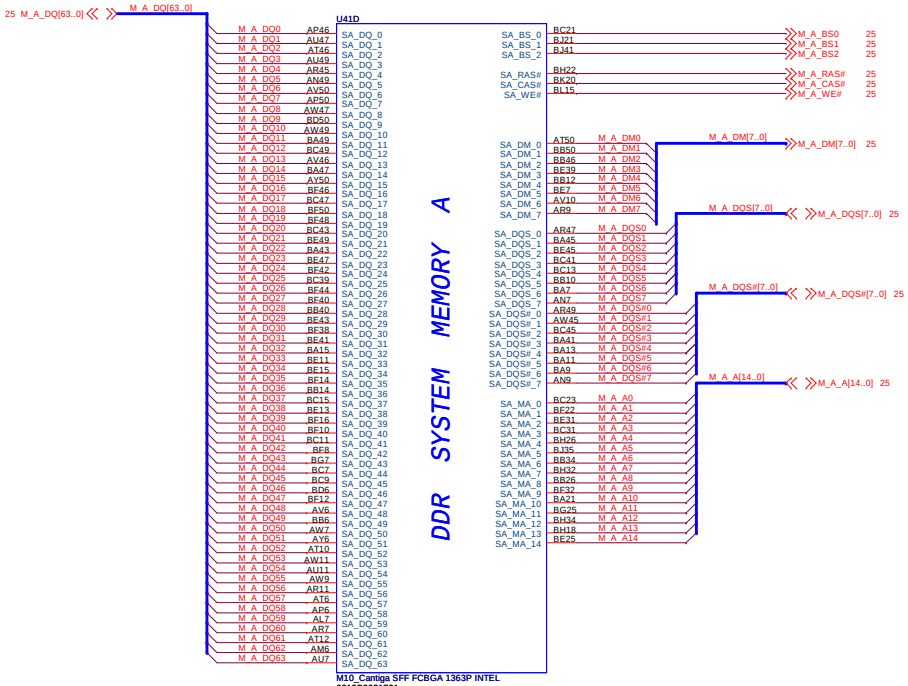
TITLE BAP41/BAP51 (Montevina SFF)

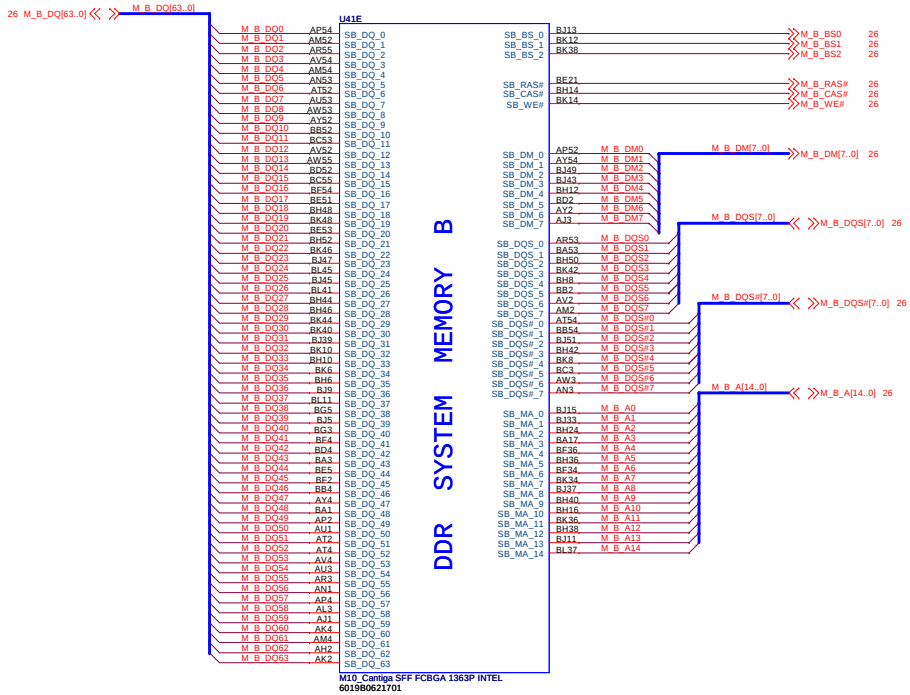
Cantiga DMI/Graph2/6)

SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A229001-ALG	A02

SHEET 19 of 49

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009





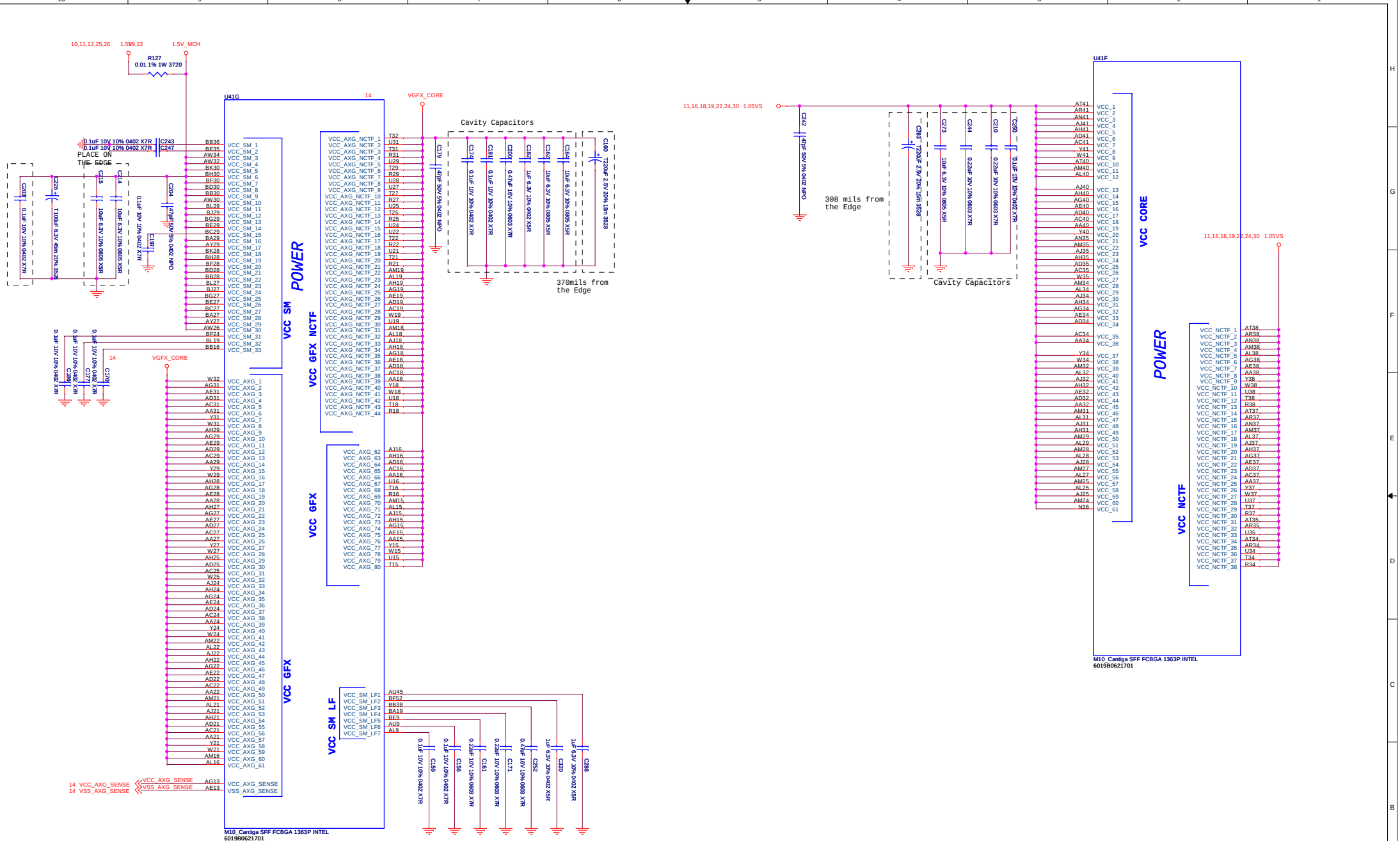
CHANGE by	Shiun-Chin Chang	DATE	Wednesday, July 01, 2009

INVENTEC

TITLE
BAP41/BAP51 (Montevina SFF)
Cantiga DDR3(3/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A229001-ALG	A02

SHEET 20 of 49



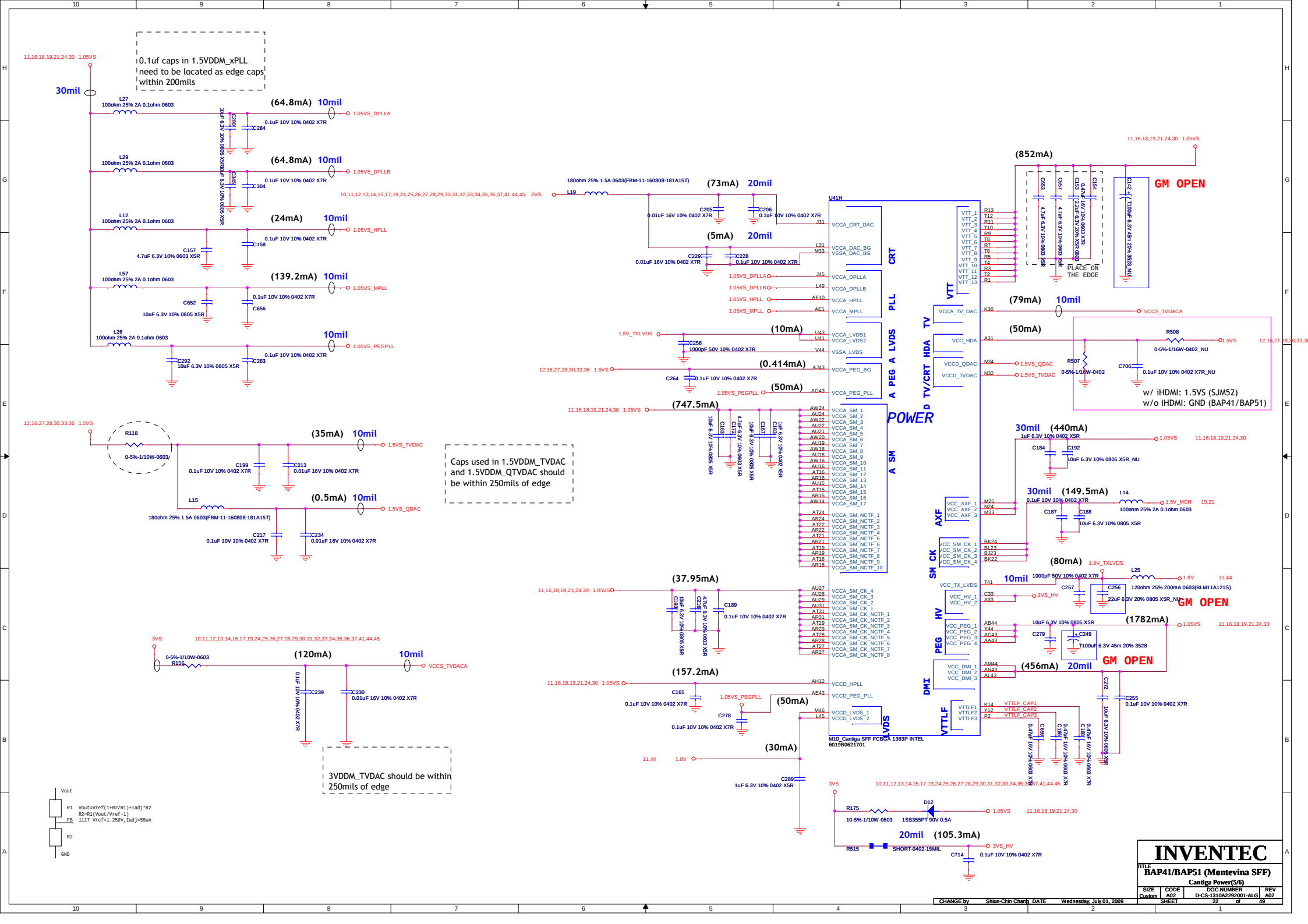
CHANGE by	Shiun-Chin Chang	DATE	Wednesday, July 01, 2009

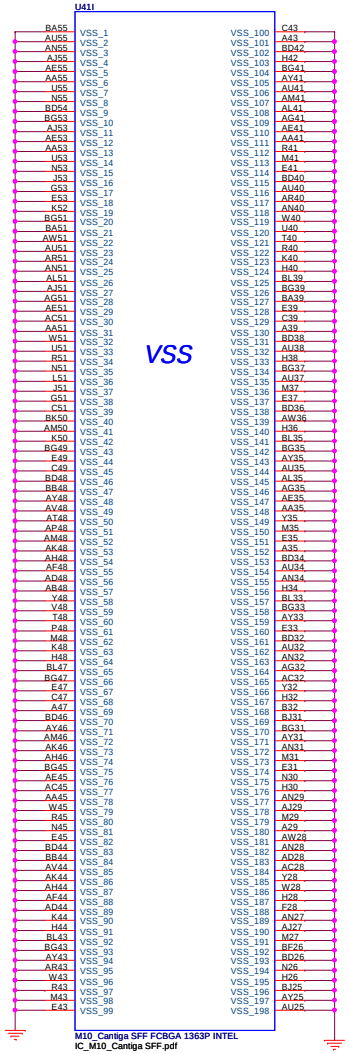
INVENTEC

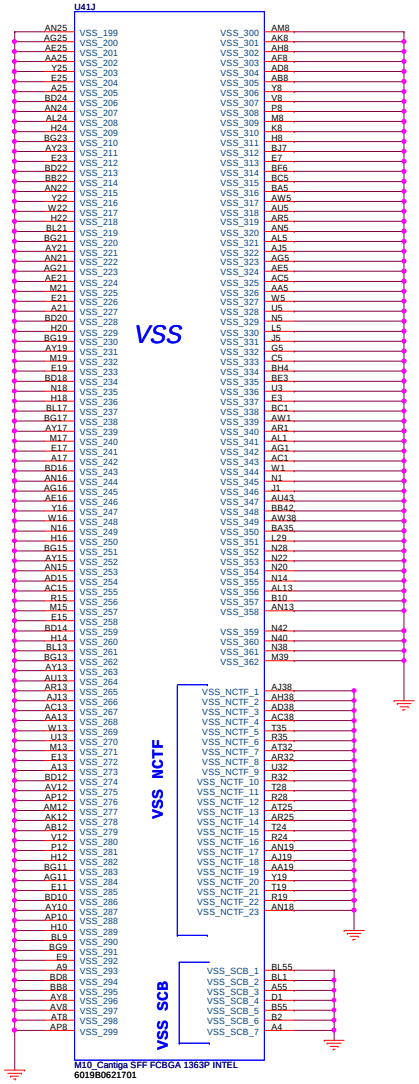
TITLE
BAP41/BAP51 (Montevina SFF)
Cantiga Power(4/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A229001-ALG	A02

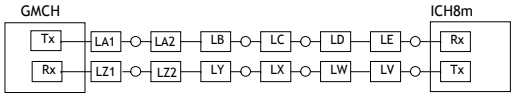
SHEET 21 of 49


0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge
3VDDM_TVDAC should be within 250mils of edge
POWER
U41H
M10_Cantiga SFF FCBGA 1363P INTEL 6019B0621701
GM OPEN
PLACE ON THE EDGE
w/ iHDMI: 1.5VS (SJM52)
w/o iHDMI: GND (BAP41/BAP51)
INVENTEC
BAP41/BAP51 (Montevina SFF)
Cantiga Power(5/6)
SIZE Custom
CODE A02
DOC.NUMBER D-CS-1310A229001-ALG
REV A02
SHEET 22 of 49
CHANGE by Shiun-Chin Chang
DATE Wednesday, July 01, 2009





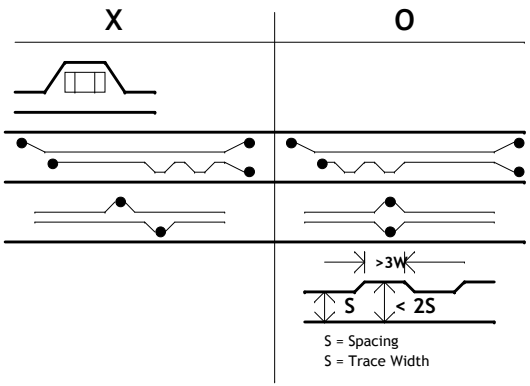
DMI Routing Guideline



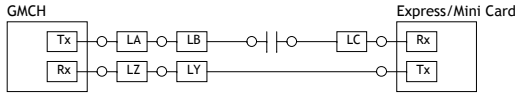
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LY (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



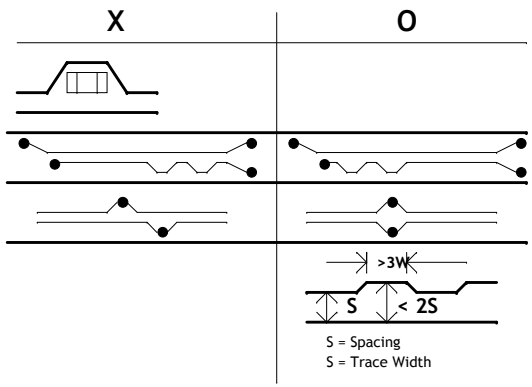
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



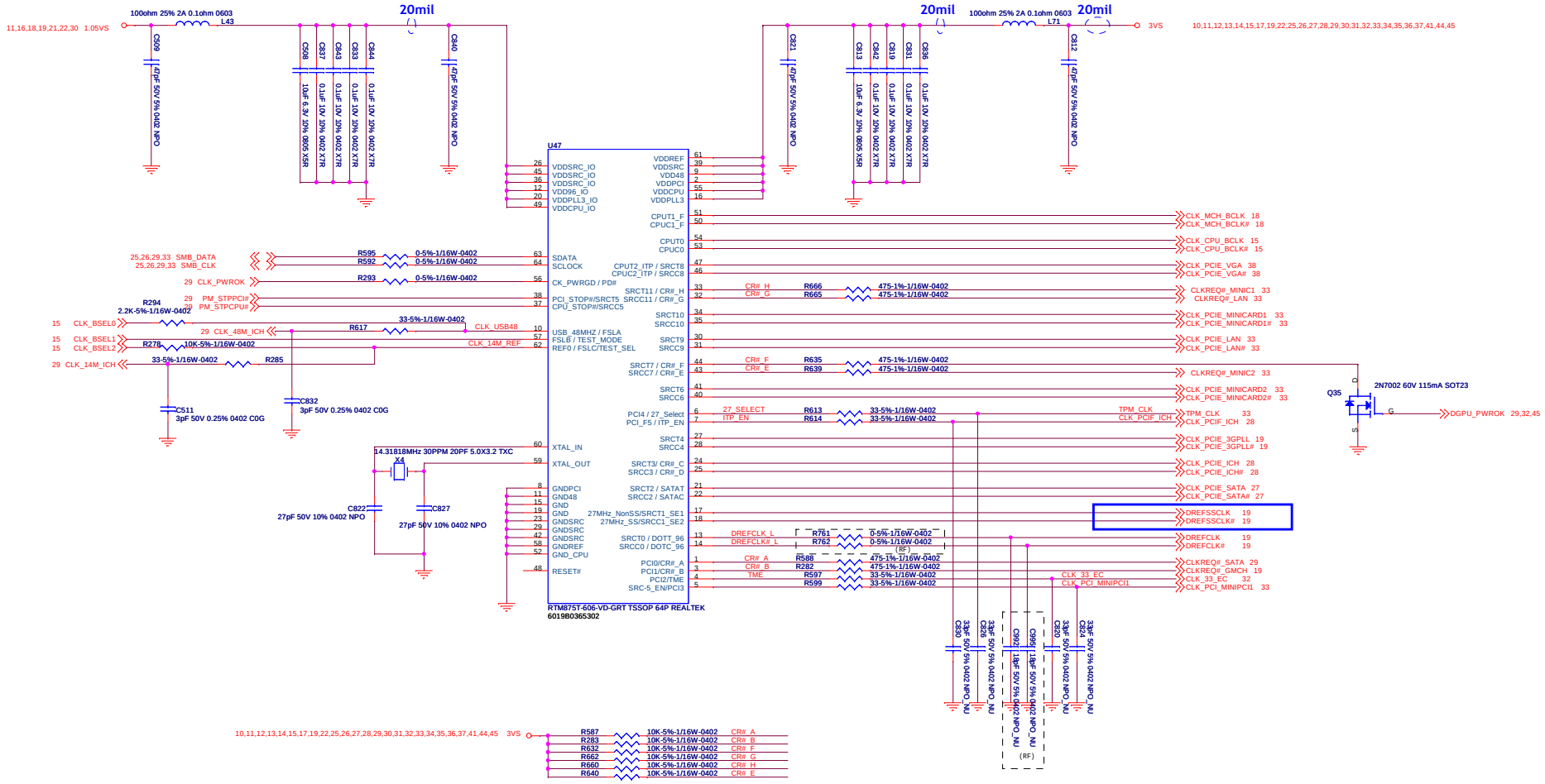
INVENTEC

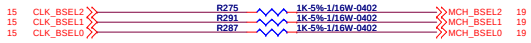
TITLE BAP41/BAP51 (Montevina SFF)
Cantiga Ground(6/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

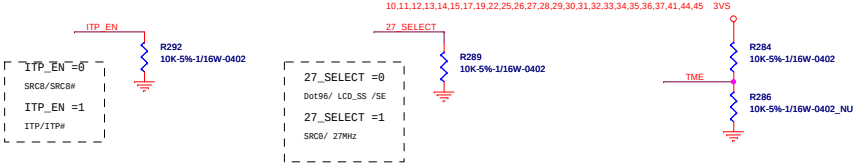
SHEET 23 of 49

CHANGE by Shiun-Chin Chang DATE Monday, June 29, 2009





FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *



CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

INVENTEC

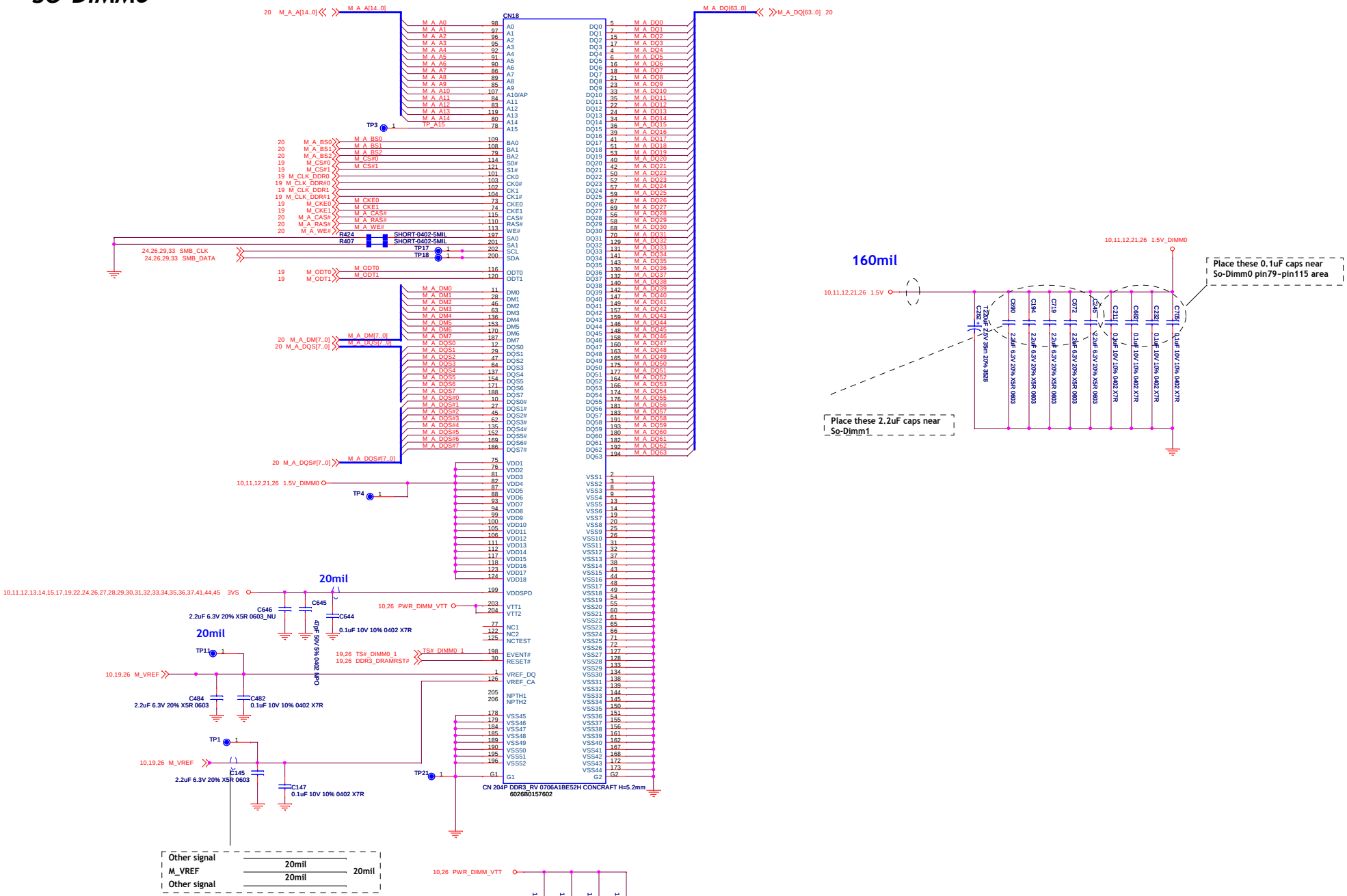
TITLE BAP41/BAP51 (Montevina SFF)

Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009 SHEET 24 of 49

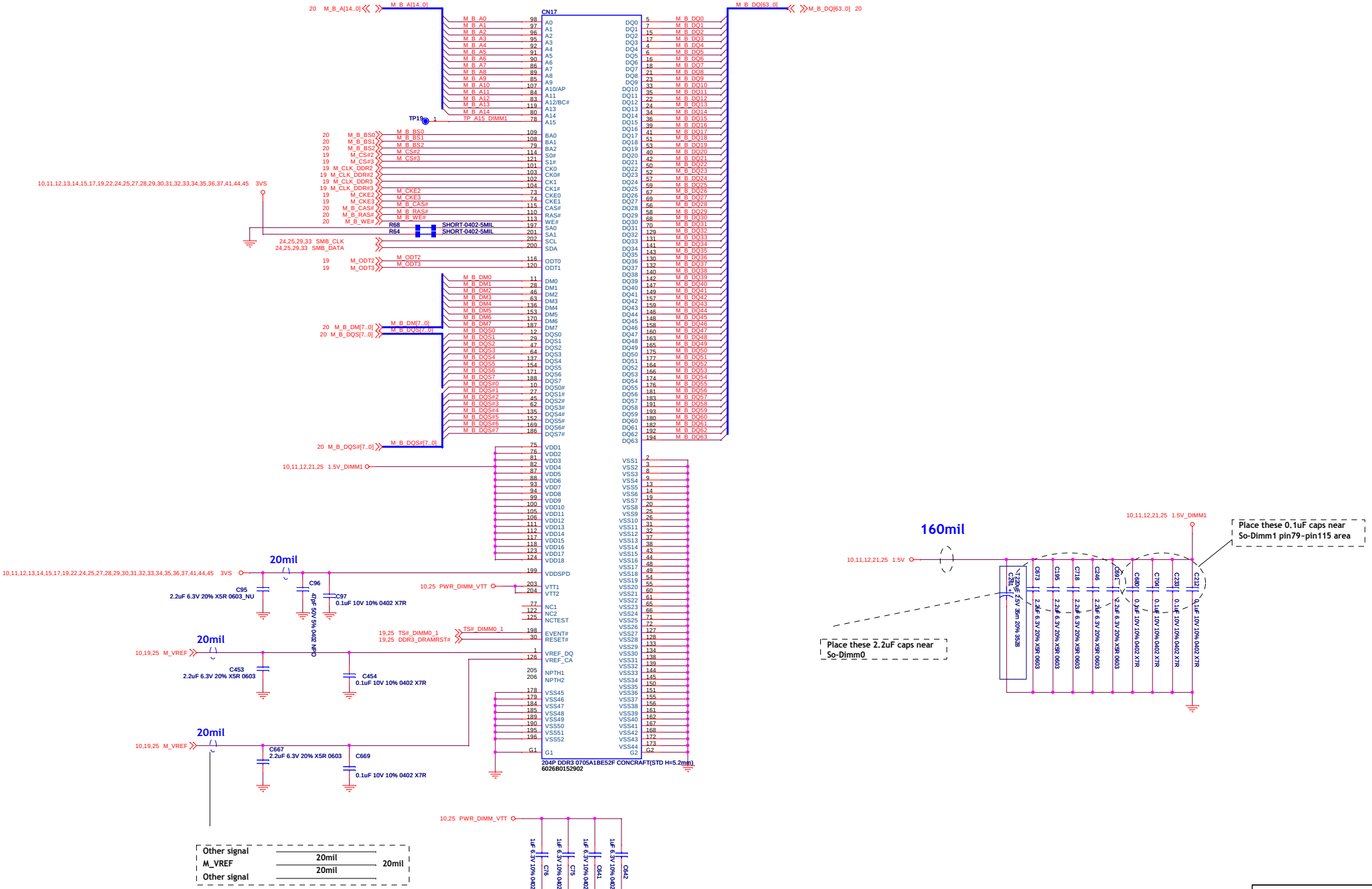
SO-DIMM0



INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) DDR3 SDRAM SO-DIMM0			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
		SHEET 25 of 49	

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009

SO-DIMM1



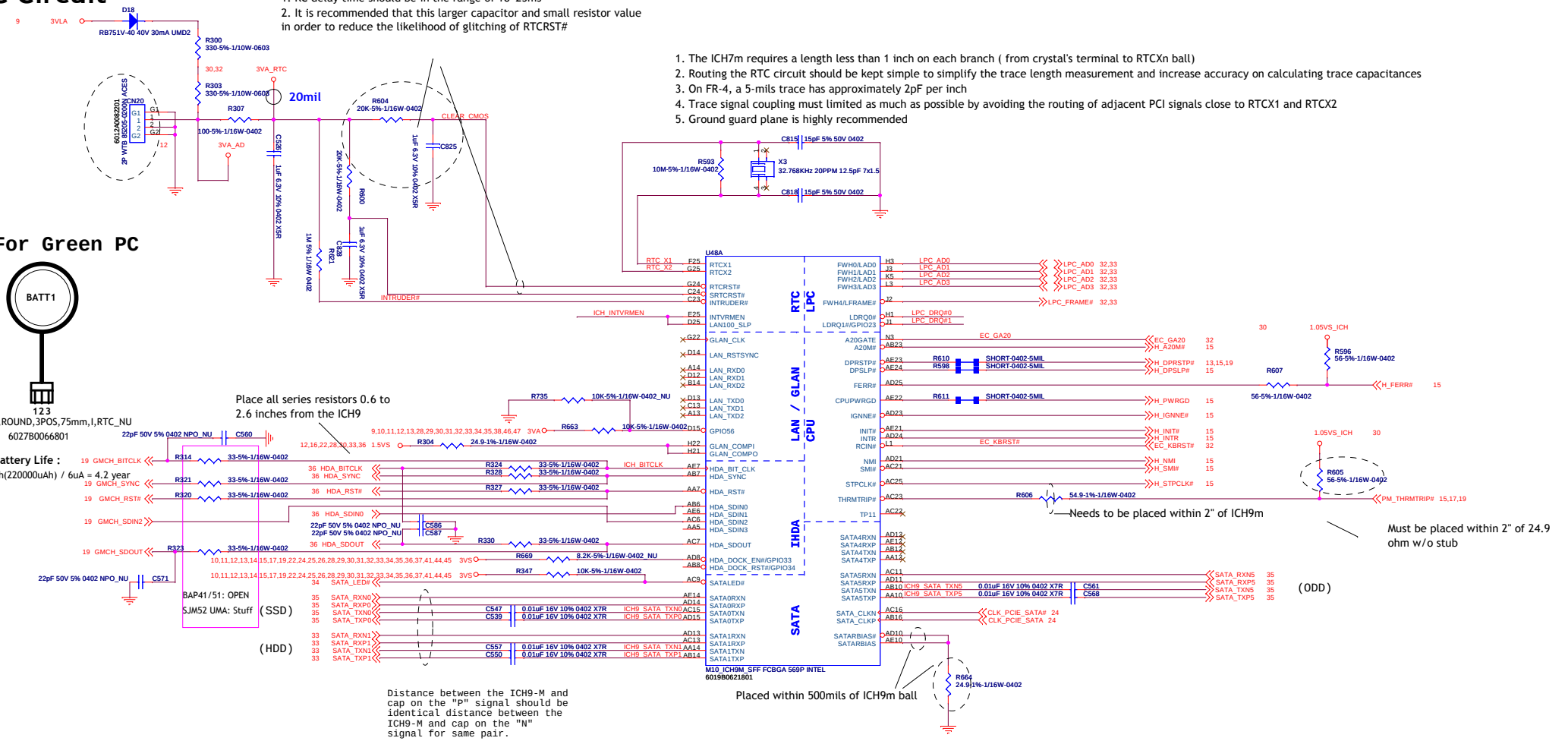
INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) DDR3 SDRAM SO-DIMM1			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
		SHEET 26 of 49	

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



	Enable	Disable
INTVRMEN	1(Default)	0

XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

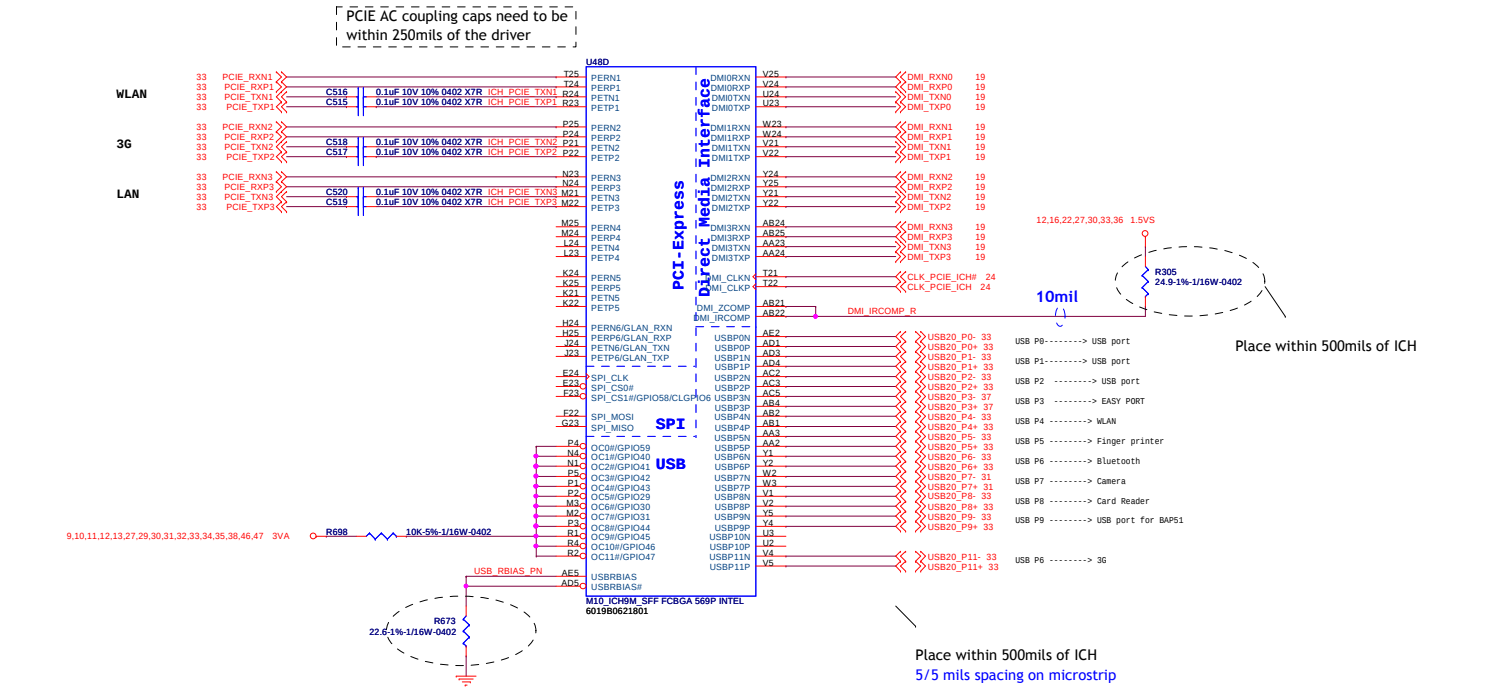
INVENTEC

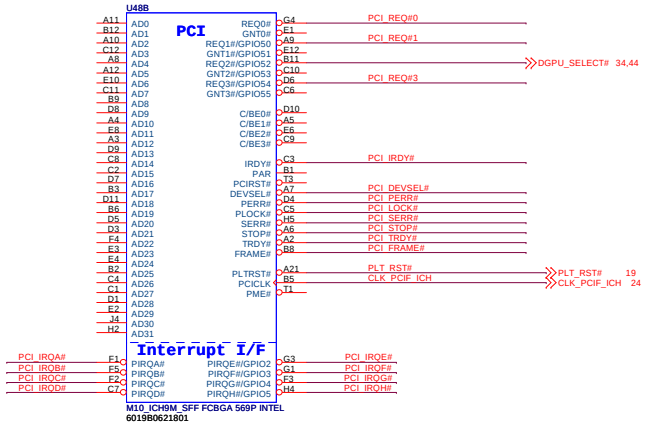
TITLE: BAP41/BAP51 (Montevina SFF)
ICH9M CPU/SATA(1/4)

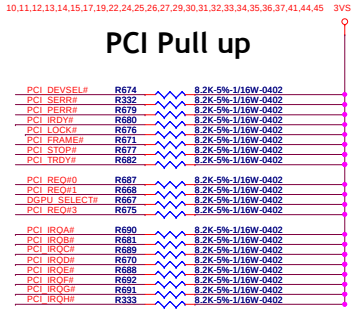
SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-AL G	A02

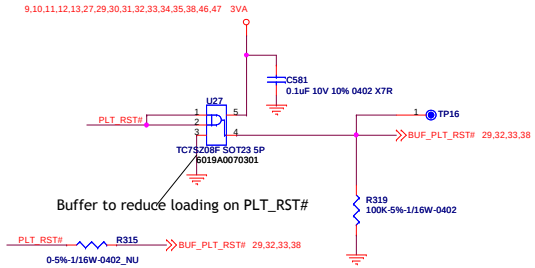
SHEET 27 of 49

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009









PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

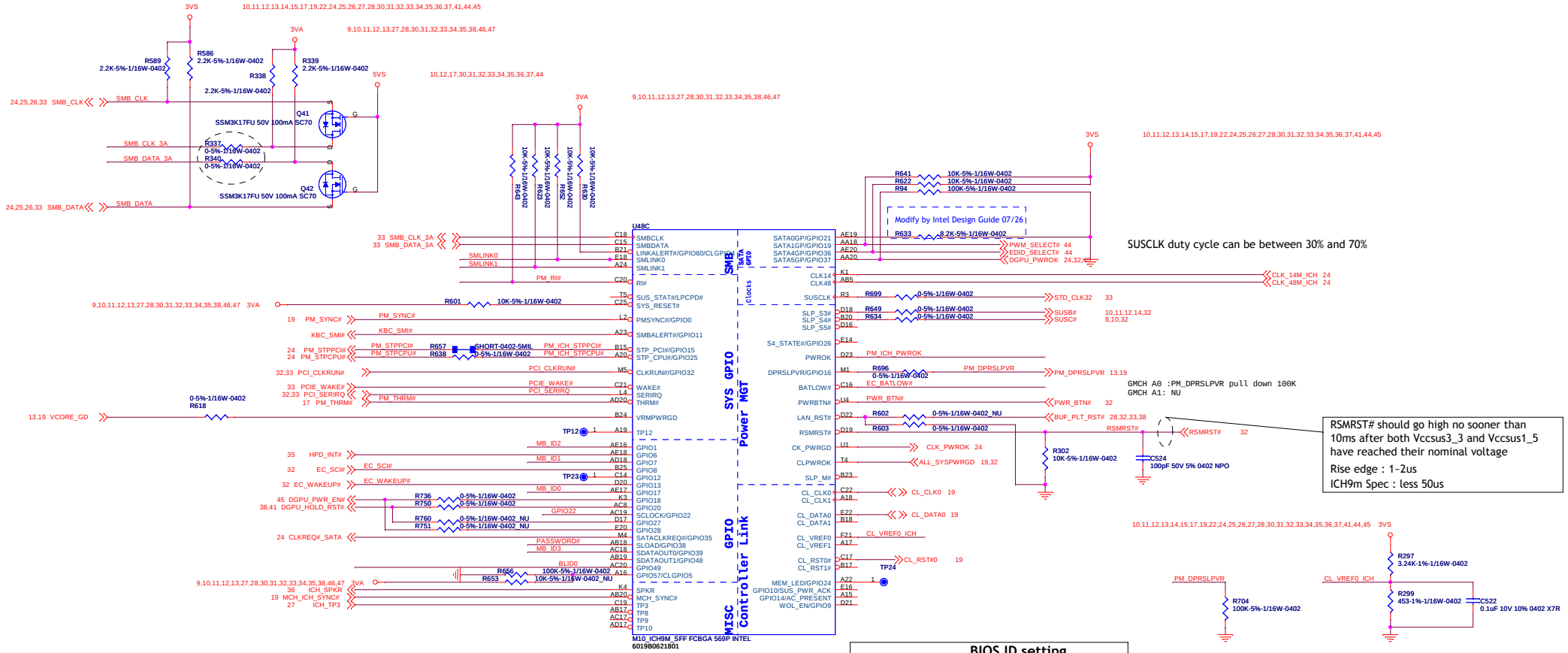
INVENTEC

TITLE BAP41/BAP51 (Montevina SFF)

ICH9M PCI/PCIE/DMI/USB(2/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A229001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009 SHEET 28 of 49



BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
BAP41 (UMA)	1	1	0	0
BAP51 (UMA)	1	0	1	1
JM31 (dGPU)	1	0	1	0
SJM31 (dGPU)	1	0	0	1
BAP31 (dGPU)	1	0	0	0
BAP41 (dGPU)	0	1	1	1
BAP51 (dGPU)	0	1	1	0
SJM52 (UMA)	0	1	0	1
SJM52 (dGPU)	0	1	0	0
BAP52 (UMA)	0	0	1	1
BAP52 (dGPU)	0	0	1	0
BXP41(UMA/dGPU)	0	0	0	1
X	0	0	0	0

ICH9m strap

ACZ_SPKR	No stuff : by default Stuff : For NO reboot

ICH_SPKR R695 1K-5%-1/16W-0402_NU

GPIO22 R637 10K-5%-1/16W-0402

R642 0-5%-1/16W-0402_NU

Default is OPEN
Add 0ohm for BIOS Recovery

PMU P/U

EC_WAKEUP#	R301	10K-5%-1/16W-0402
EC_SCI#	R615	10K-5%-1/16W-0402
EC_BATLOW#	R661	8.2K-5%-1/16W-0402
PCIE_WAKE#	R631	1K-5%-1/16W-0402
KBC_SMI#	R624	10K-5%-1/16W-0402
PCI_SERIRQ	R714	8.2K-5%-1/16W-0402
PM_THRM#	R619	8.2K-5%-1/16W-0402
PCI_CLKRUN#	R713	8.2K-5%-1/16W-0402
MB_ID0	R651	10K-5%-1/16W-0402
MB_ID3	R655	10K-5%-1/16W-0402_NU
MB_ID2	R659	10K-5%-1/16W-0402
MB_ID1	R646	10K-5%-1/16W-0402
BLID0	R608	10K-5%-1/16W-0402_NU
DGPU_PWR_EN#	R331	10K-5%-1/16W-0402
MB_ID3	R654	10K-5%-1/16W-0402
MB_ID2	R658	10K-5%-1/16W-0402_NU
MB_ID0	R650	10K-5%-1/16W-0402_NU
MB_ID1	R645	10K-5%-1/16W-0402_NU
PM_STPPCI#	R310	10K-5%-1/16W-0402_NU
PM_STPCPU#	R308	10K-5%-1/16W-0402_NU

PASSWORD CLEAR

R625 10K-5%-1/16W-0402

PASSWORD#

C838 1uF 10V 10% X5R 0402_NU

ERASE PASSWORD

Please close to door

INVENTEC

TITLE BAP41/BAP51 (Montevina SFF)
ICH9M GPIO(3/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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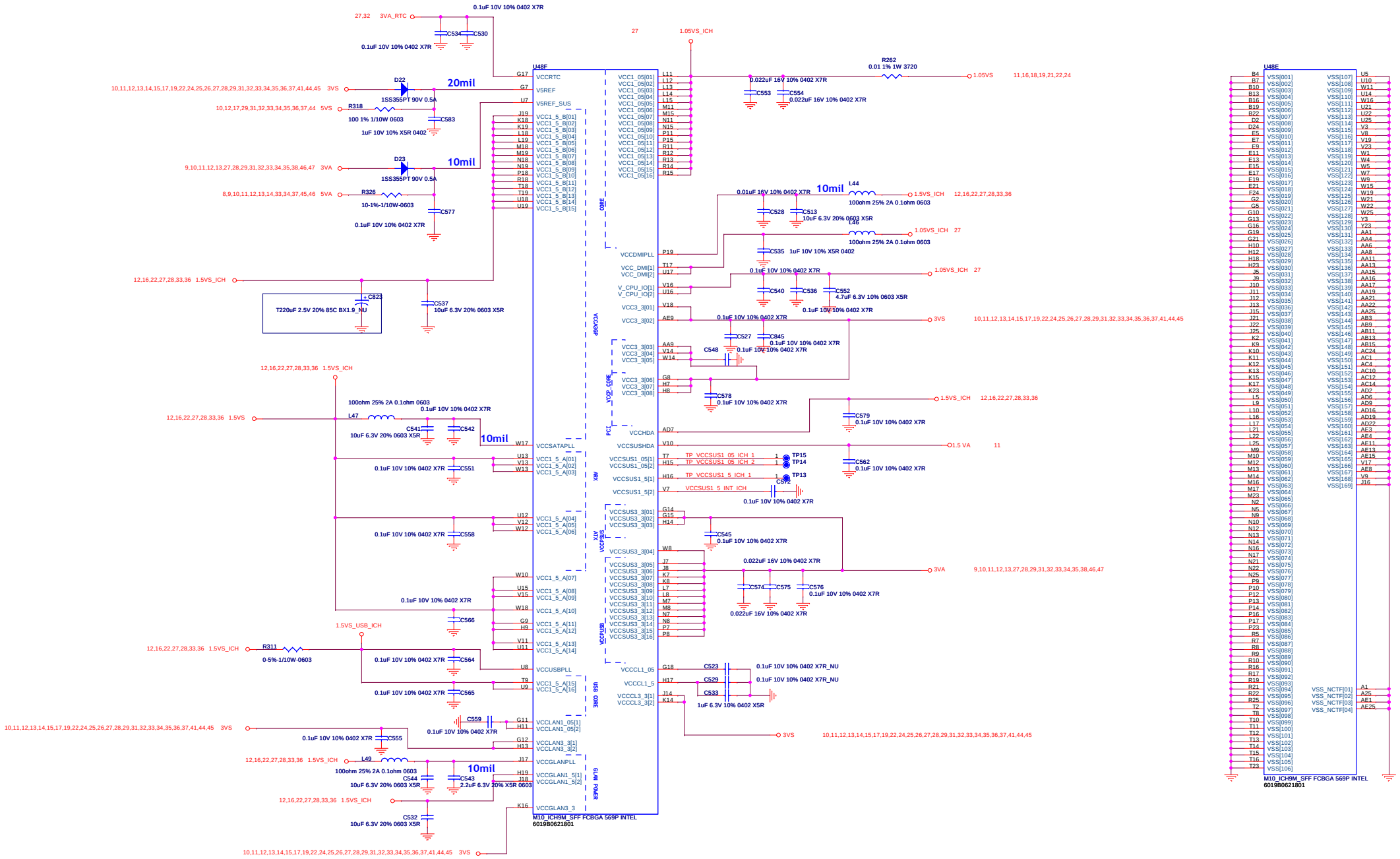
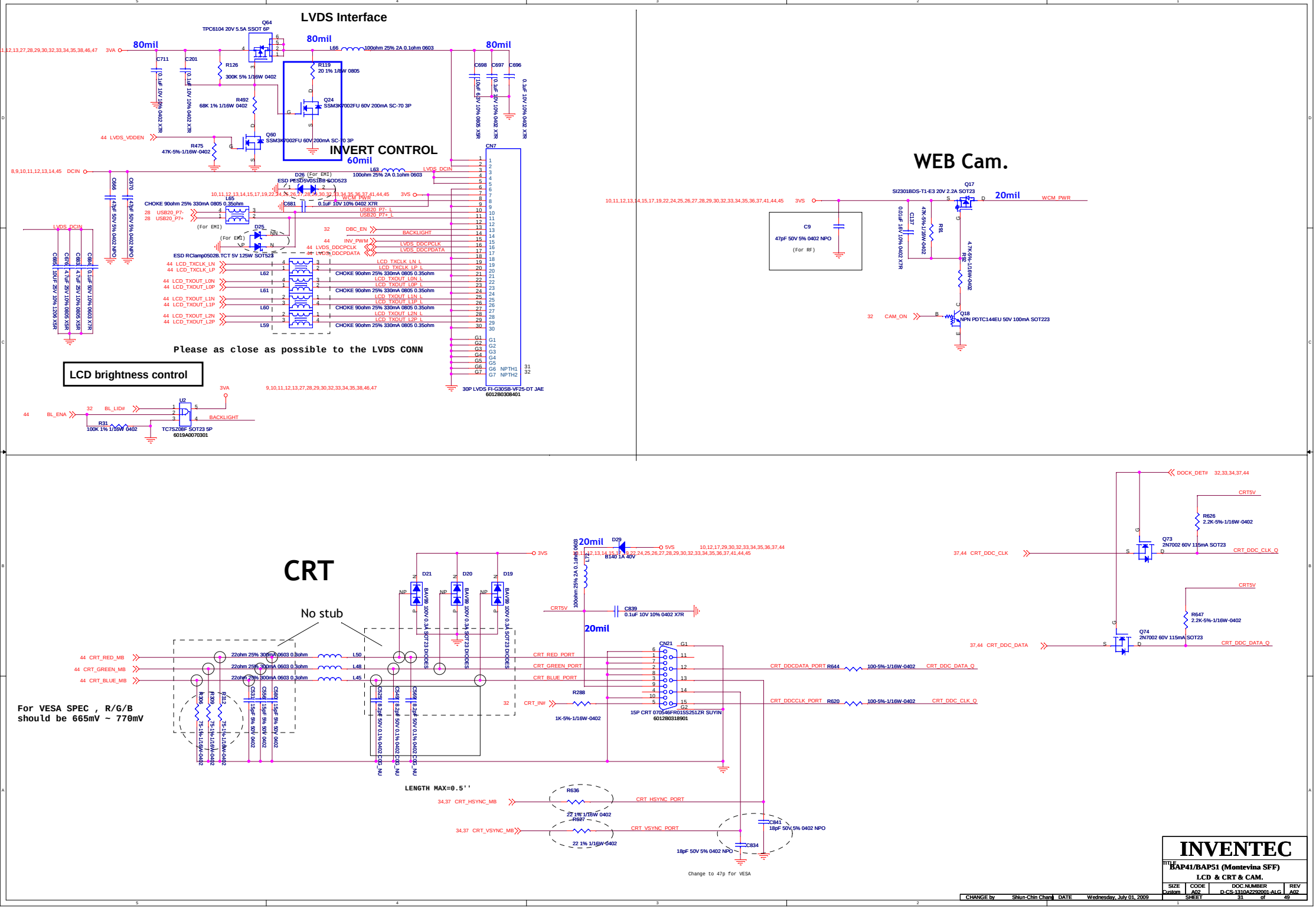
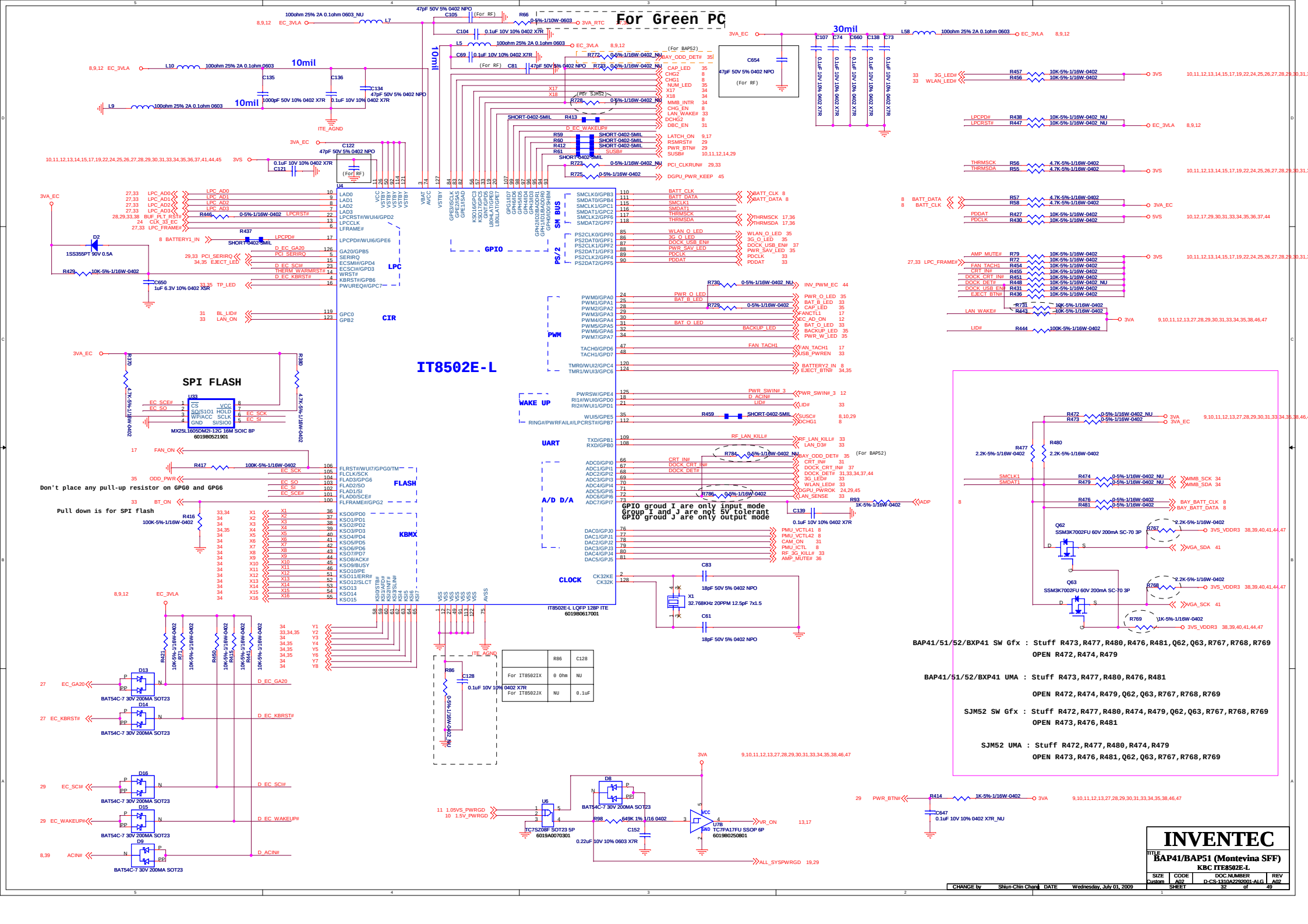
CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009



INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF)			
ICH9M Power/GND(4/4)			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
CHANGE by Shiun-Chin Chang	DATE Wednesday, July 01, 2009	SHEET 30 of 49	


LVDS Interface
INVERT CONTROL
WEB Cam.
CRT
LCD brightness control
Please as close as possible to the LVDS CONN
No stub
For VESA SPEC , R/G/B should be 665mV ~ 770mV
LENGTH MAX=0.5''
Change to 47p for VESA
30P LVDS FI-G30SB-VF25-DT JAE 6012B0308401
15P CRT 070546FR015S251ZR SUYIN 6012B0318901
TC7SZ08F SOT23 5P 6019A0070301
SI2301BDS-T1-E3 20V 2.2A SOT23
NPN PDTC144EU 50V 100mA SOT223
Q73 2N7002 60V 115mA SOT23
Q74 2N7002 60V 115mA SOT23
INVENTEC
BAP41/BAP51 (Montevina SFF)
LCD & CRT & CAM.
Custom
A02
D-CS-1310A229201-ALG
A02
CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009
SHEET 31 of 49


For Green PC
IT8502E-L
IT8502E-L LQFP 128P ITE
6019B0617001
SPI FLASH
MX25L16065DM2I-12G 16M SOIC 8P
6019B0521901
Don't place any pull-up resistor on GPG0 and GPG6
Pull down is for SPI flash
GPIO groud I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode
BAP41/51/52/BXP41 SW Gfx : Stuff R473,R477,R480,R476,R481,Q62,Q63,R767,R768,R769
OPEN R472,R474,R479
BAP41/51/52/BXP41 UMA : Stuff R473,R477,R480,R476,R481
OPEN R472,R474,R479,Q62,Q63,R767,R768,R769
SJM52 SW Gfx : Stuff R472,R477,R480,R474,R479,Q62,Q63,R767,R768,R769
OPEN R473,R476,R481
SJM52 UMA : Stuff R472,R477,R480,R474,R479
OPEN R473,R476,R481,Q62,Q63,R767,R768,R769
INVENTEC
BAP41/BAP51 (Montevina SFF)
KBC ITE8502E-L
SIZE Custom
CODE A02
DOC.NUMBER D-CS-1310A2292001-ALG
REV A02
CHANGE by Shiun-Chin Chang
DATE Wednesday, July 01, 2009
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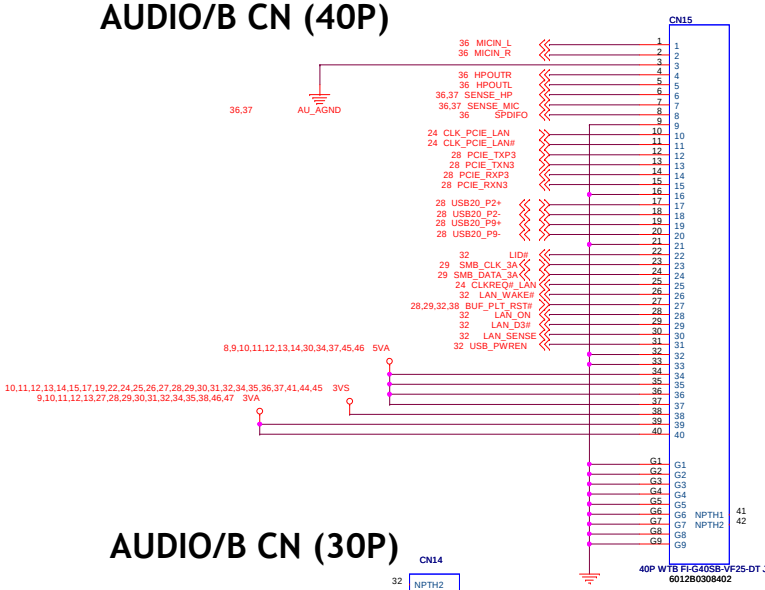
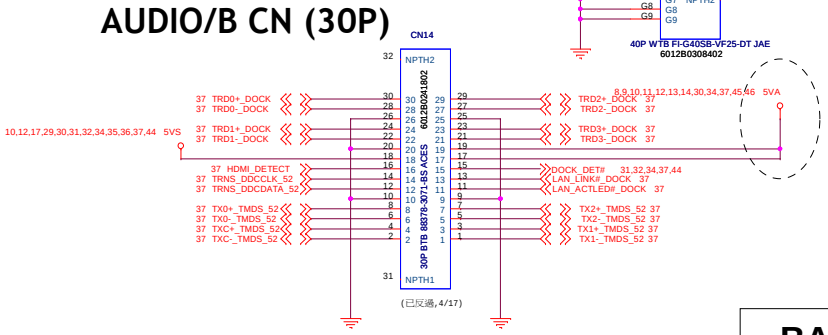
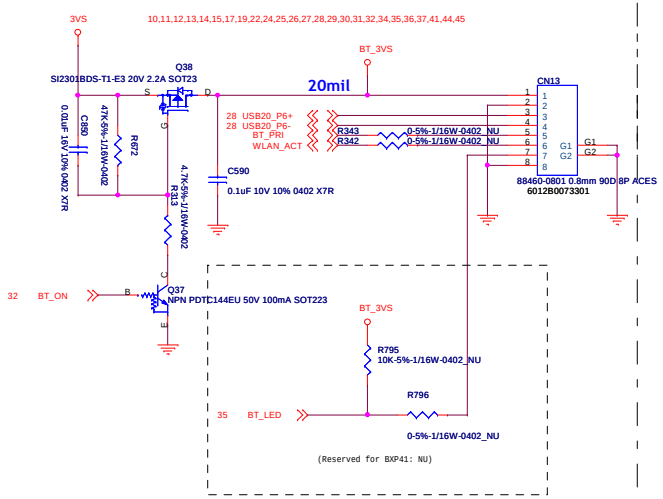
AUDIO/B CN (40P)



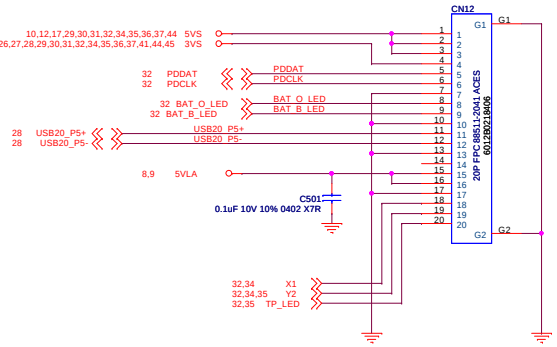
AUDIO/B CN (30P)



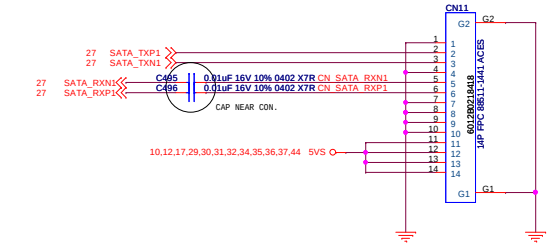
Bluetooth CN



GLIDE PAD Board

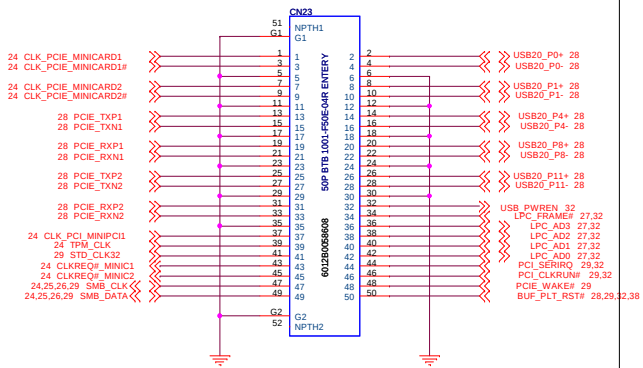


HDD BOARD CN



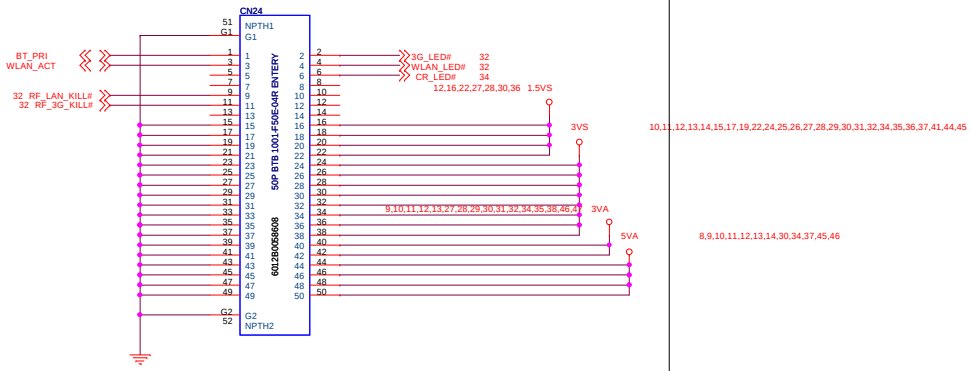
BAP41/BXP41:
Transfer/B CN:6012B0058608

BAP51/52/SJM52:
Mini-Card/B CN:6012B0058609



BAP41/BXP41:
Transfer/B CN:6012B0058608

BAP51/52/SJM52:
Mini-Card/B CN:6012B0058609



INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) Daughter Connector			
SIZE Custom	CODE A02	DOC NUMBER D-CS-1310A2292001-ALG	REV A02
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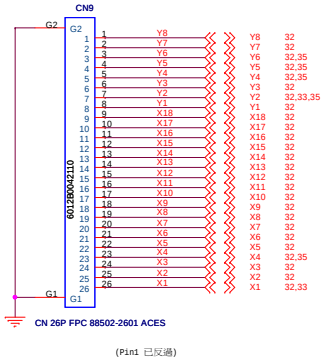
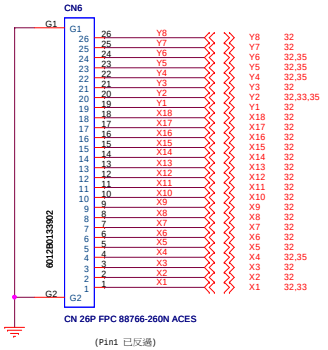
CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009

To K/B(For BAP41)

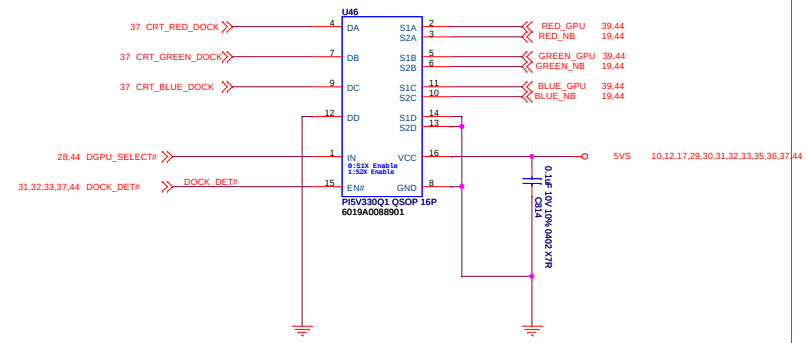


To K/B (For BAP51/BAP52/SJM52)

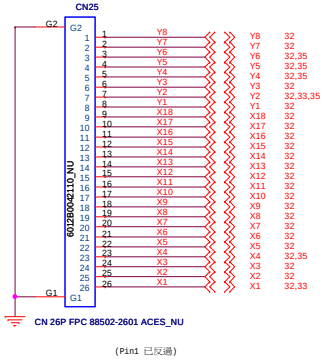


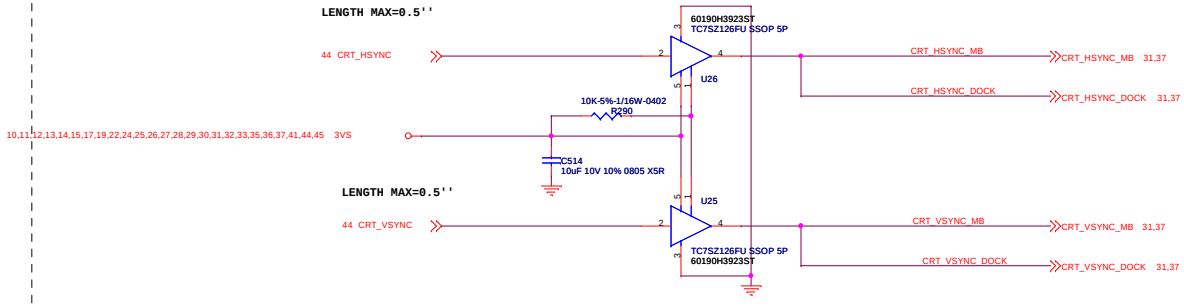
BAP41/51/52/BXP41: Stuff U46,C814

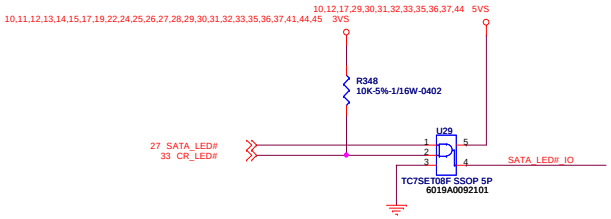
SJM52 : OPEN U46,C814



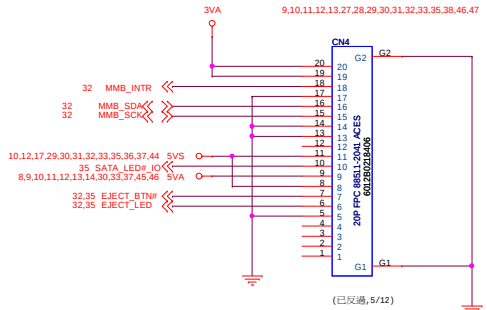
To K/B(For BXP41)







SW Sensor BOARD(For SJM52)



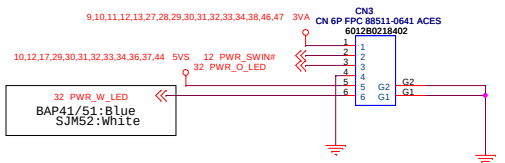
BAP41/51/52/BXP41: OPEN

SJM52: Stuff

INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) BDP			
SIZE Custom	CODE A02	DOC NUMBER D-CS-1310A2292001-ALG	REV A02
		SHEET 34 of 49	

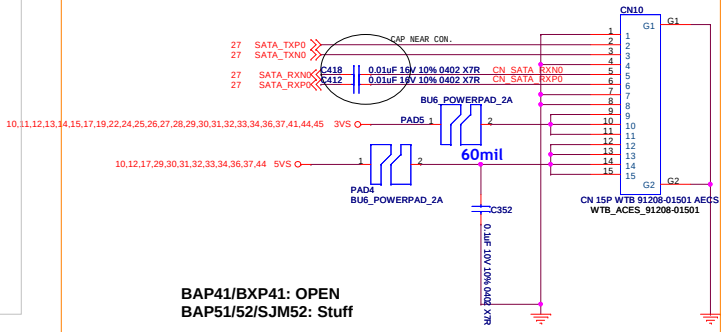
CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009

MB(PWR_SWIN#) TO DC-JACK/B



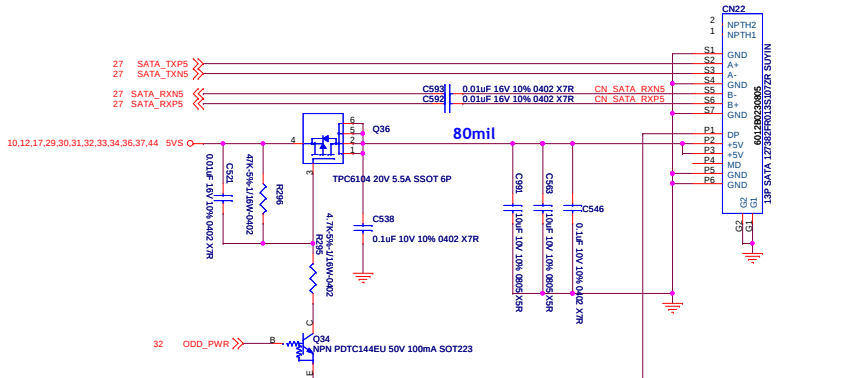
BXP41: OPEN

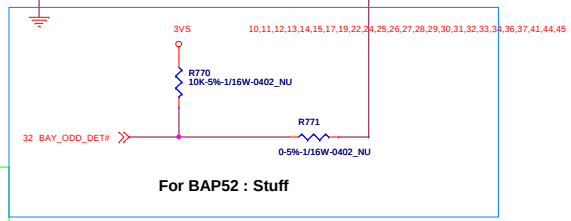
SSD I/F



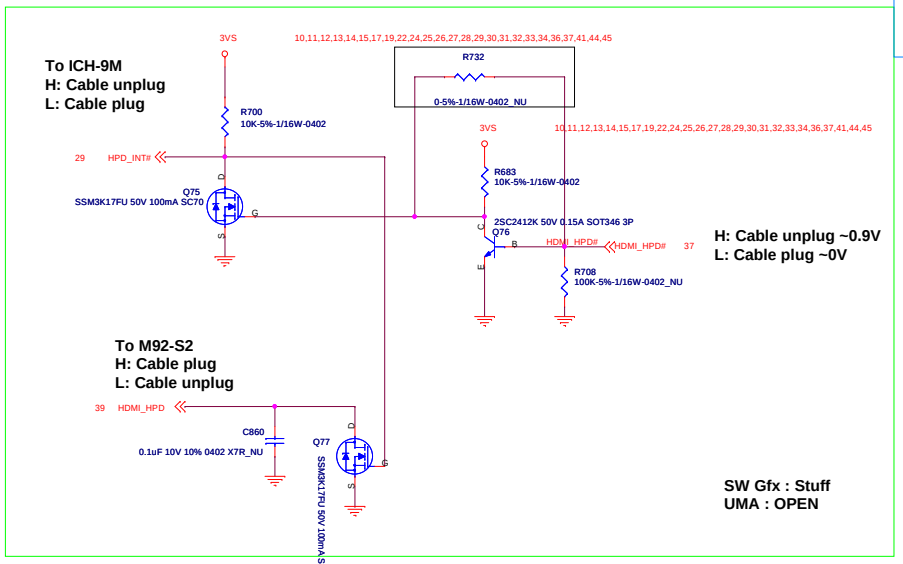
BAP41/BXP41: OPEN
BAP51/52/SJM52: Stuff

ODD I/F





For BAP52 : Stuff



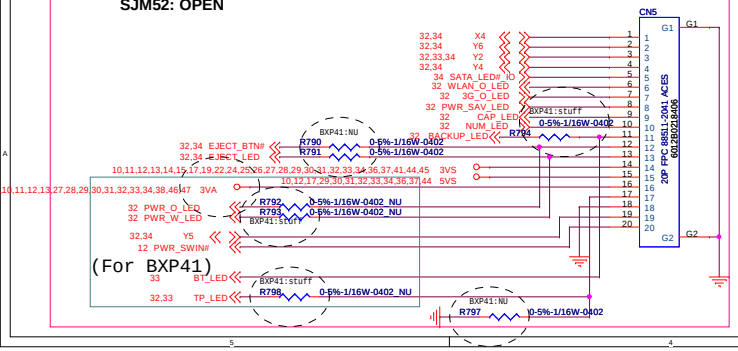
SW Gfx : Stuff
UMA : OPEN

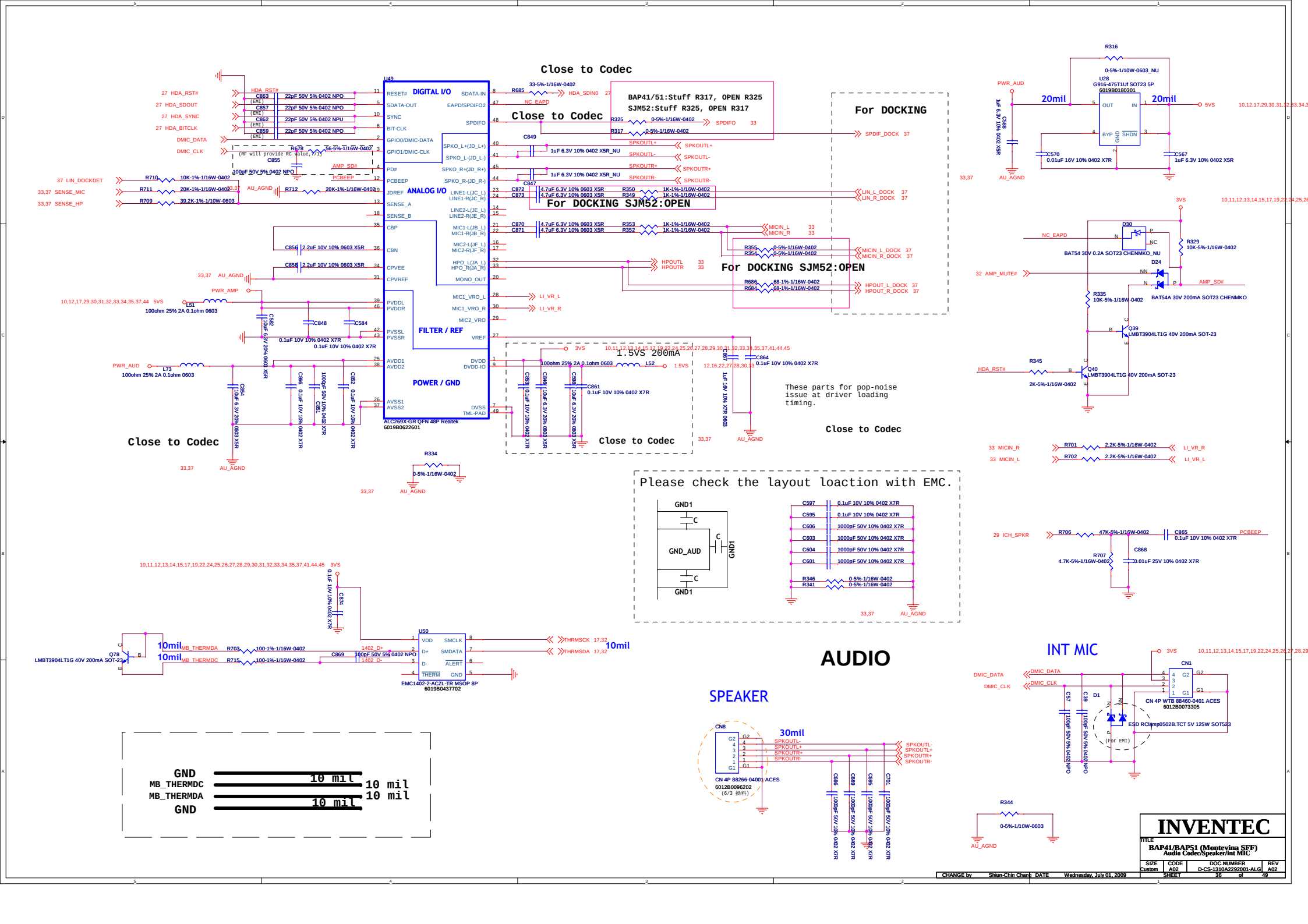
SW Gfx : OPEN
UMA : Stuff

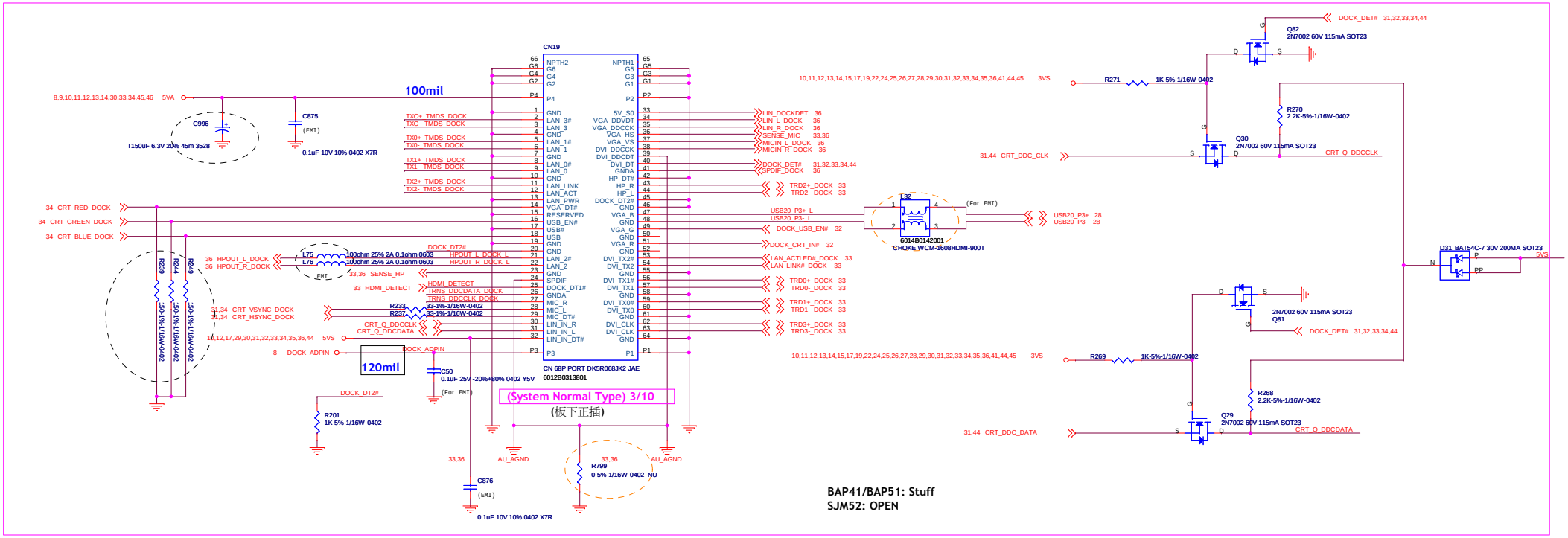
Size:0201

SW/B CN

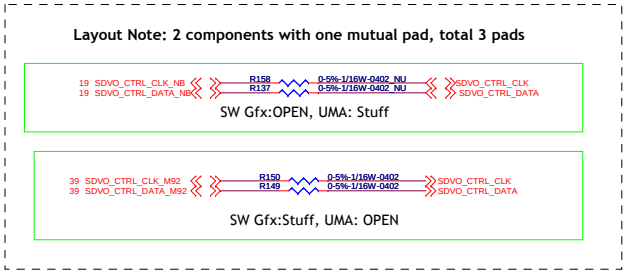
BAP41/51/52/BXP41: Stuff
SJM52: OPEN

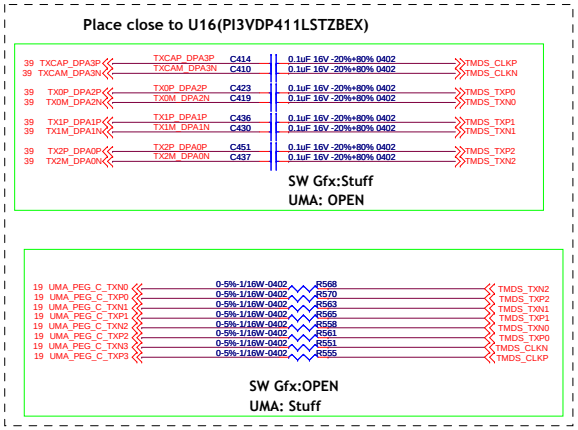


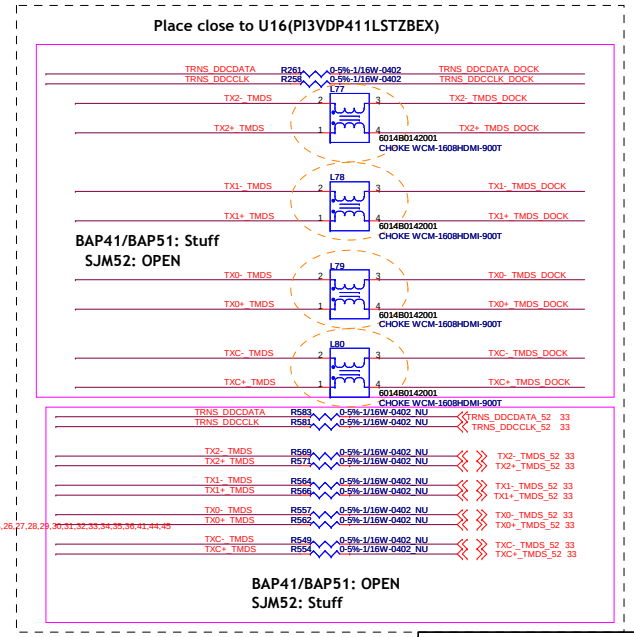

Close to Codec
U49
DIGITAL I/O
ANALOG I/O
FILTER / REF
POWER / GND
ALC269X-GR QFN 48P Realtek
6019B0622601
BAP41/51:Stuff R317, OPEN R325
SJM52:Stuff R325, OPEN R317
For DOCKING
For DOCKING SJM52:OPEN
For DOCKING SJM52:OPEN
1.5VS 200mA
These parts for pop-noise issue at driver loading timing.
Close to Codec
Please check the layout loaction with EMC.
GND1
GND_AUD
AUDIO
SPEAKER
INT MIC
U50
EMC1402-2-ACZL-TR MSOP 8P
6019B0437702
CN8
CN 4P 88266-04001 ACES
6012B0096202
CN1
CN 4P WTB 88460-0401 ACES
6012B0073305
ESD RClamp0502B.TCT 5V 125W SOT523
U28
G916-475T1Uf SOT23 5P
6019B0180301
BAT54 30V 0.2A SOT23 CHENMKO_NU
BAT54A 30V 200mA SOT23 CHENMKO
LMBT3904LT1G 40V 200mA SOT-23
GND
MB_THERMDC
MB_THERMDA
GND
10 mil
10 mil
10 mil
10 mil
INVENTEC
TITLE
BAP41/BAP51 (Montevina SFF)
Audio Codec/Speaker/Int MIC
SIZE Custom
CODE A02
DOC NUMBER D-CS-1310A2292001-ALG
REV A02
SHEET 36 of 49
CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009

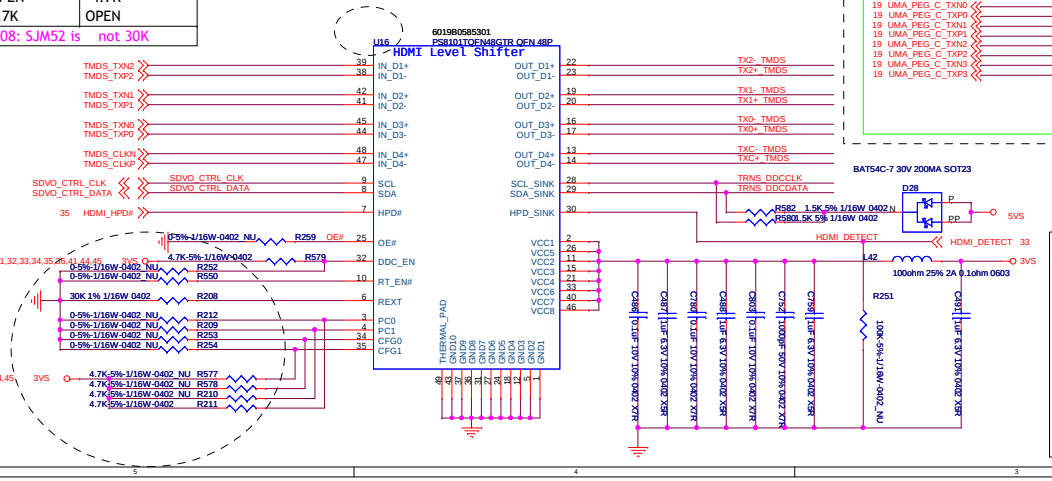


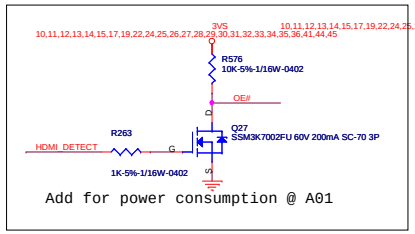
Parade	Pericom
U16 : 6019B0585301	6019B0443802
R550 : OPEN	0 ohm
R208 : 30K	OPEN
R212 : OPEN	0 ohm
R209 : OPEN	0 ohm
R253 : OPEN	0 ohm
R577 : OPEN	4.7K
R211 : 4.7K	OPEN
Note: R208: SJM52 is not 30K	









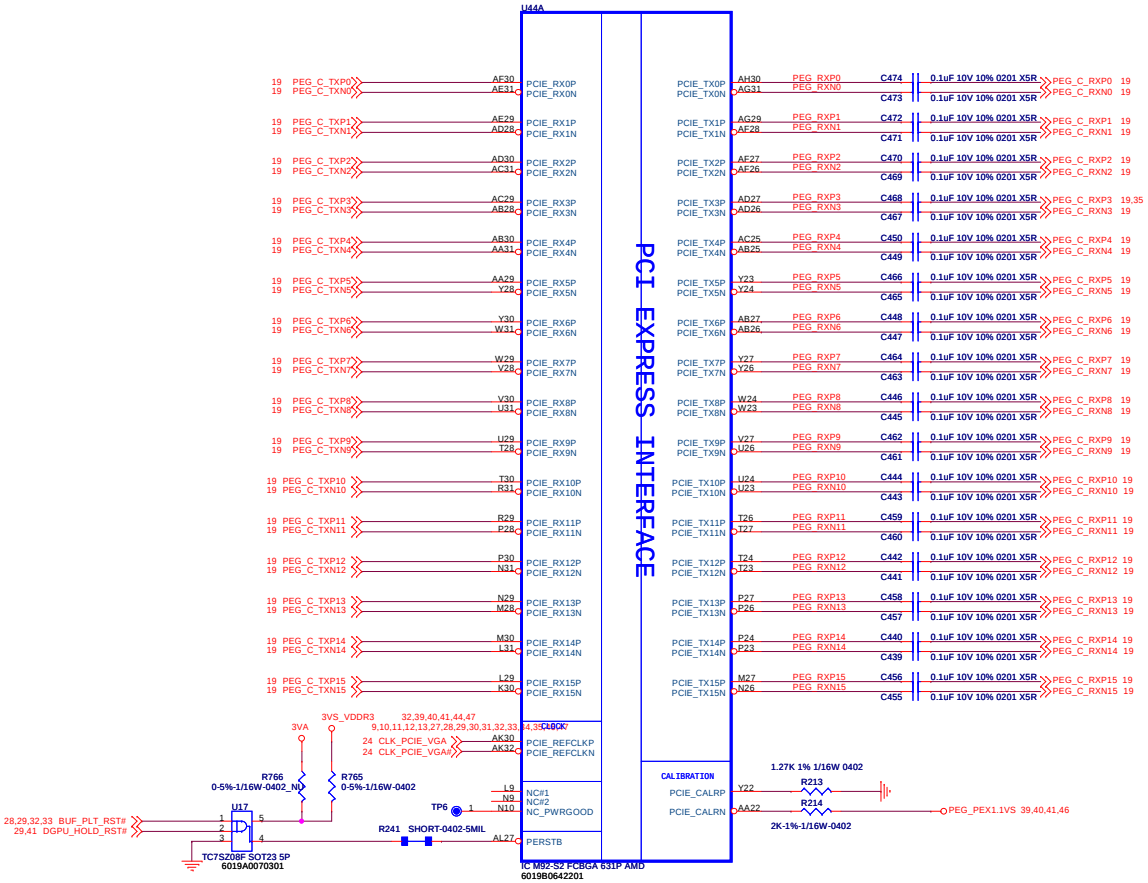


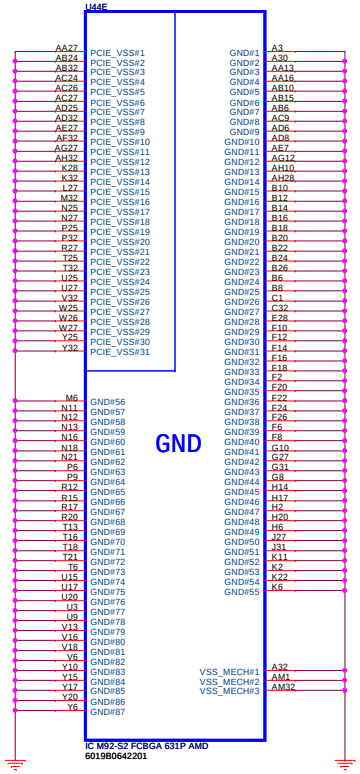
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF) EASY PORT CN/Level Shifter

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Wednesday, July 01, 2009 SHEET 37 of 49





Page 38:

SW Gfx: Stuff

UMA: OPEN

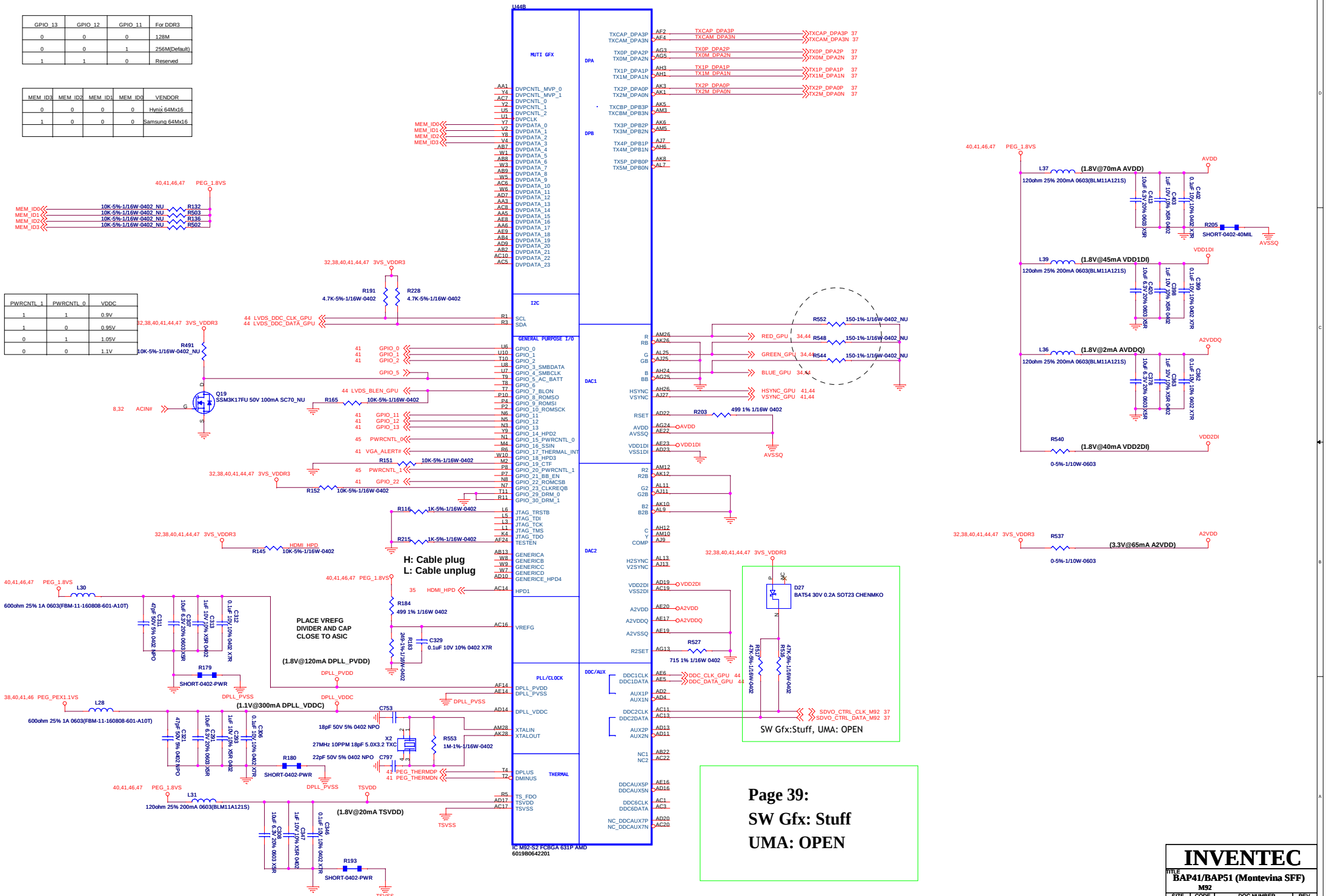
INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) M92			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
		SHEET 38 of 49	

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009

GPIO_13	GPIO_12	GPIO_11	For DDR3
0	0	0	128M
0	0	1	256M(Default)
1	1	0	Reserved

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16

PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

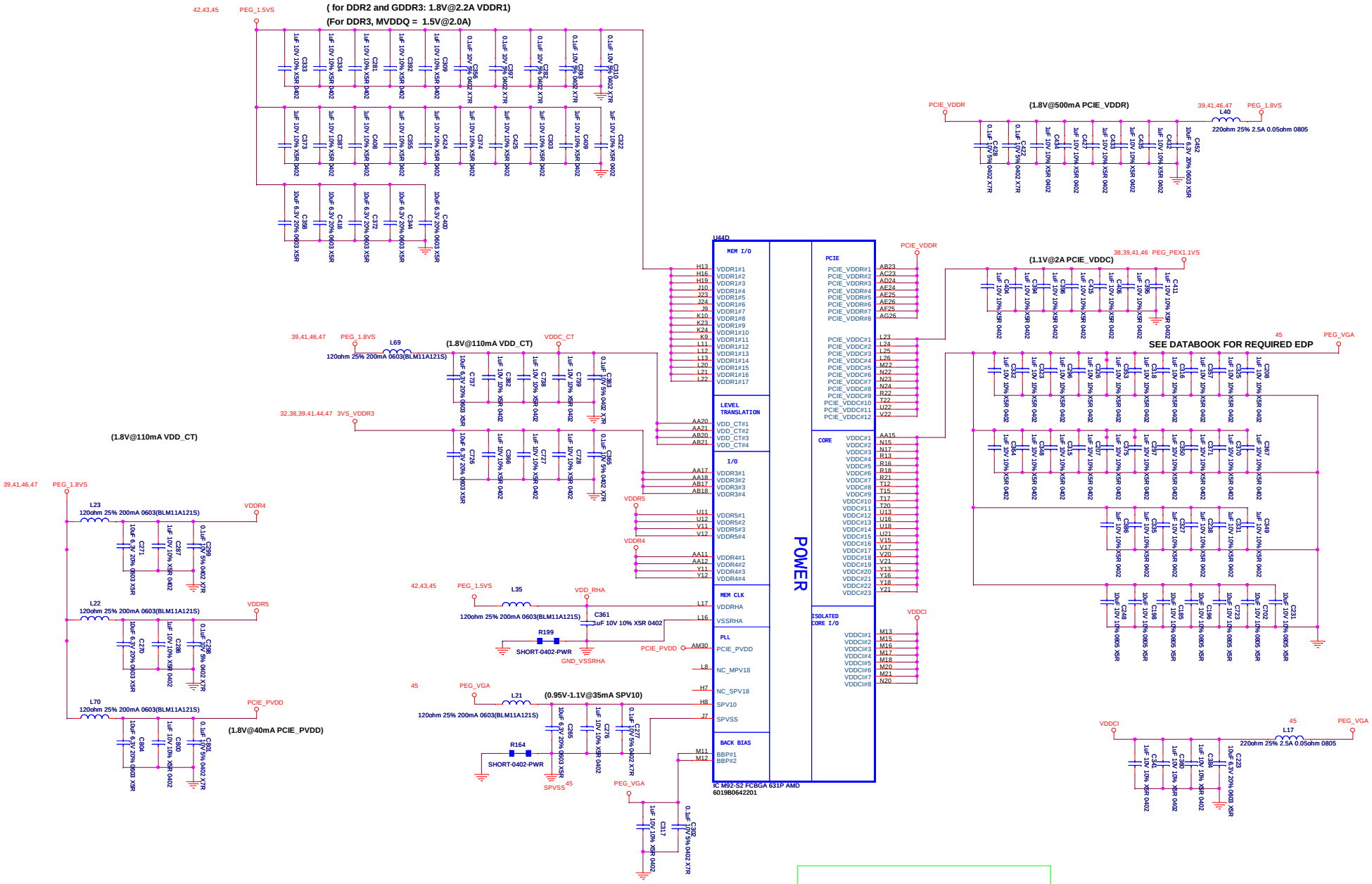


INVENTEC

TITLE BAP41/BAP51 (Montevina SFF)
M92

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009 SHEET 39 of 49



Page 40:

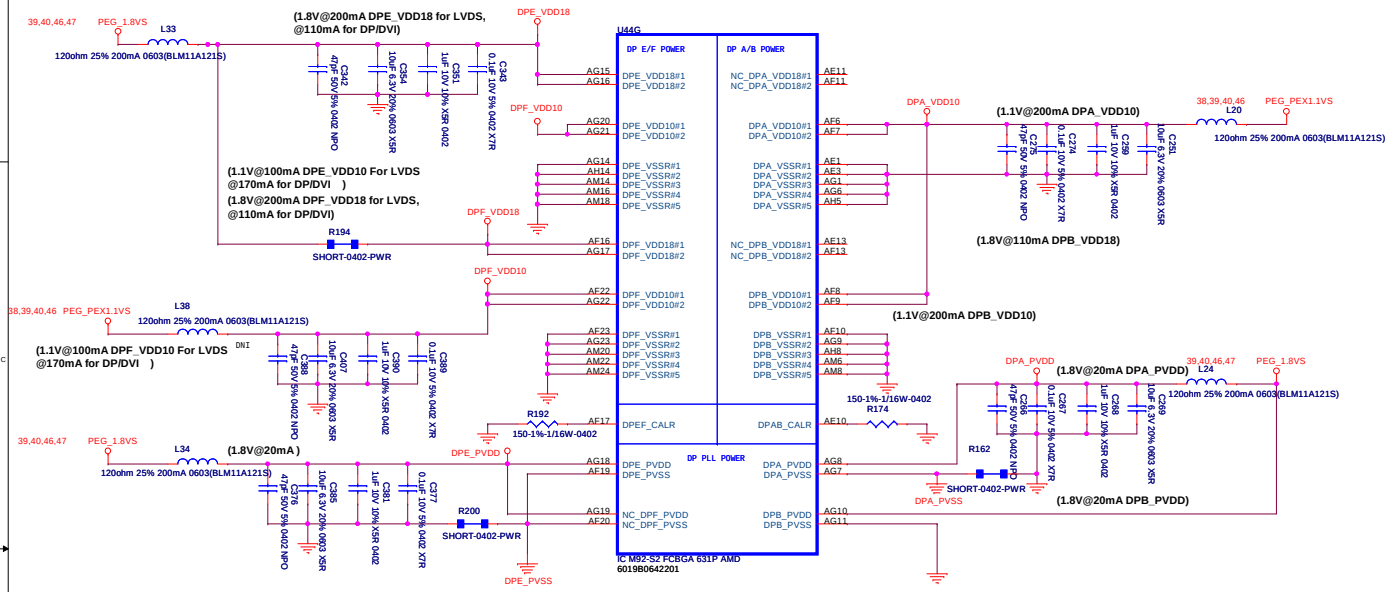
SW Gfx: Stuff

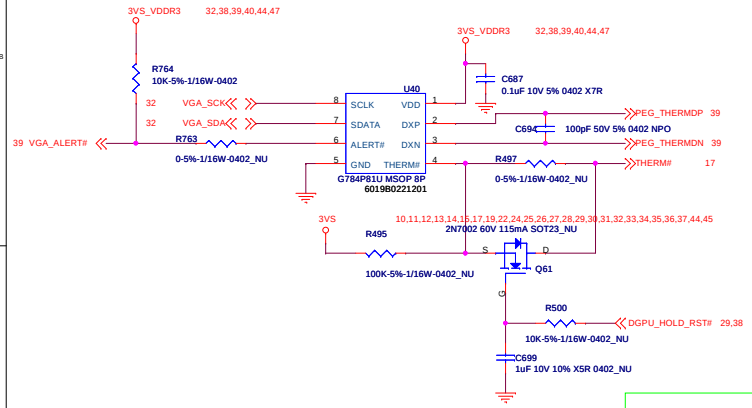
UMA: OPEN

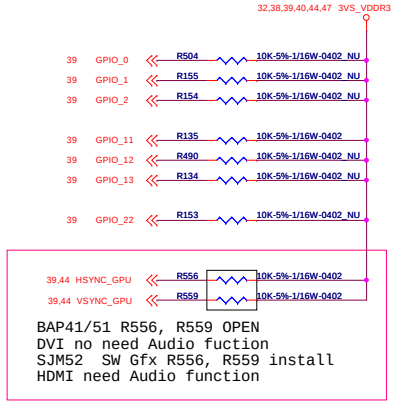
INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) M92			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
		SHEET 40 of 49	

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009

For 92, DPx_VDD10 = 1.1V
For Future ASIC, DPx_VDD10 = 1.0V







BAP41/51 R556, R559 OPEN
DVI no need Audio fuction
SJM52 SW Gfx R556, R559 install
HDMI need Audio function

PIN STRAPS

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Page 41:
SW Gfx: Stuff
UMA: OPEN

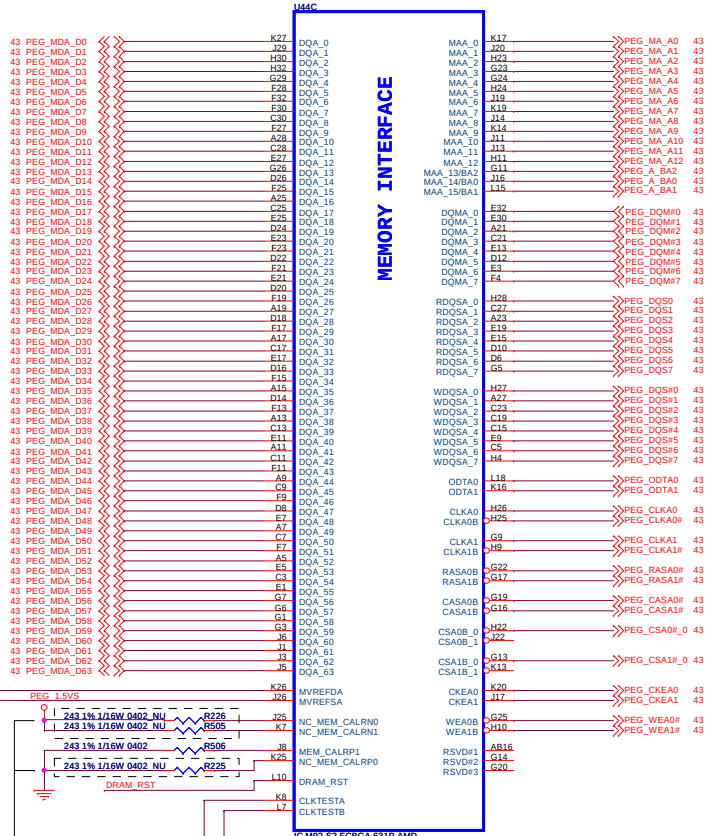
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
M92

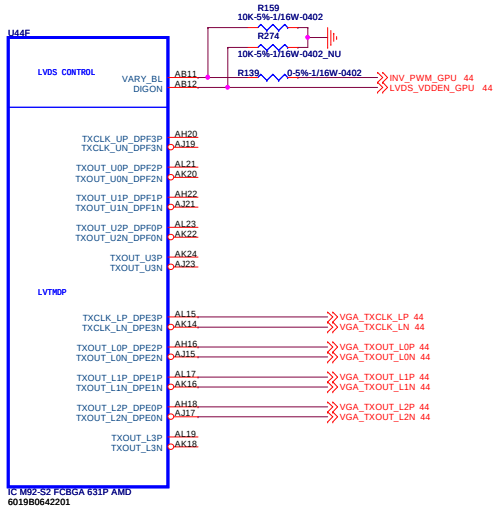
SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009 SHEET 41 of 49

DDR3 Memory Interface



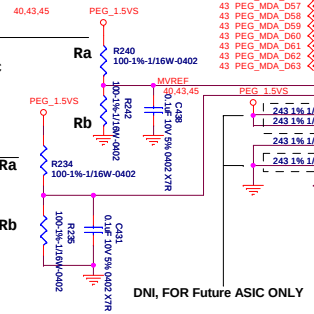
LVDS Interface



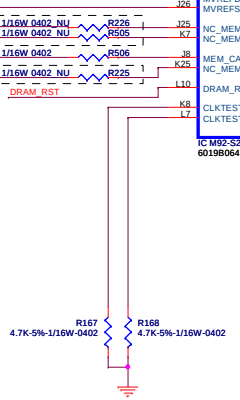
MVDDQ = 1.5V FOR DDR3 Memory

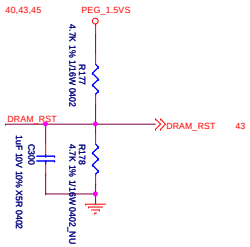
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R



DNI, FOR Future ASIC ONLY

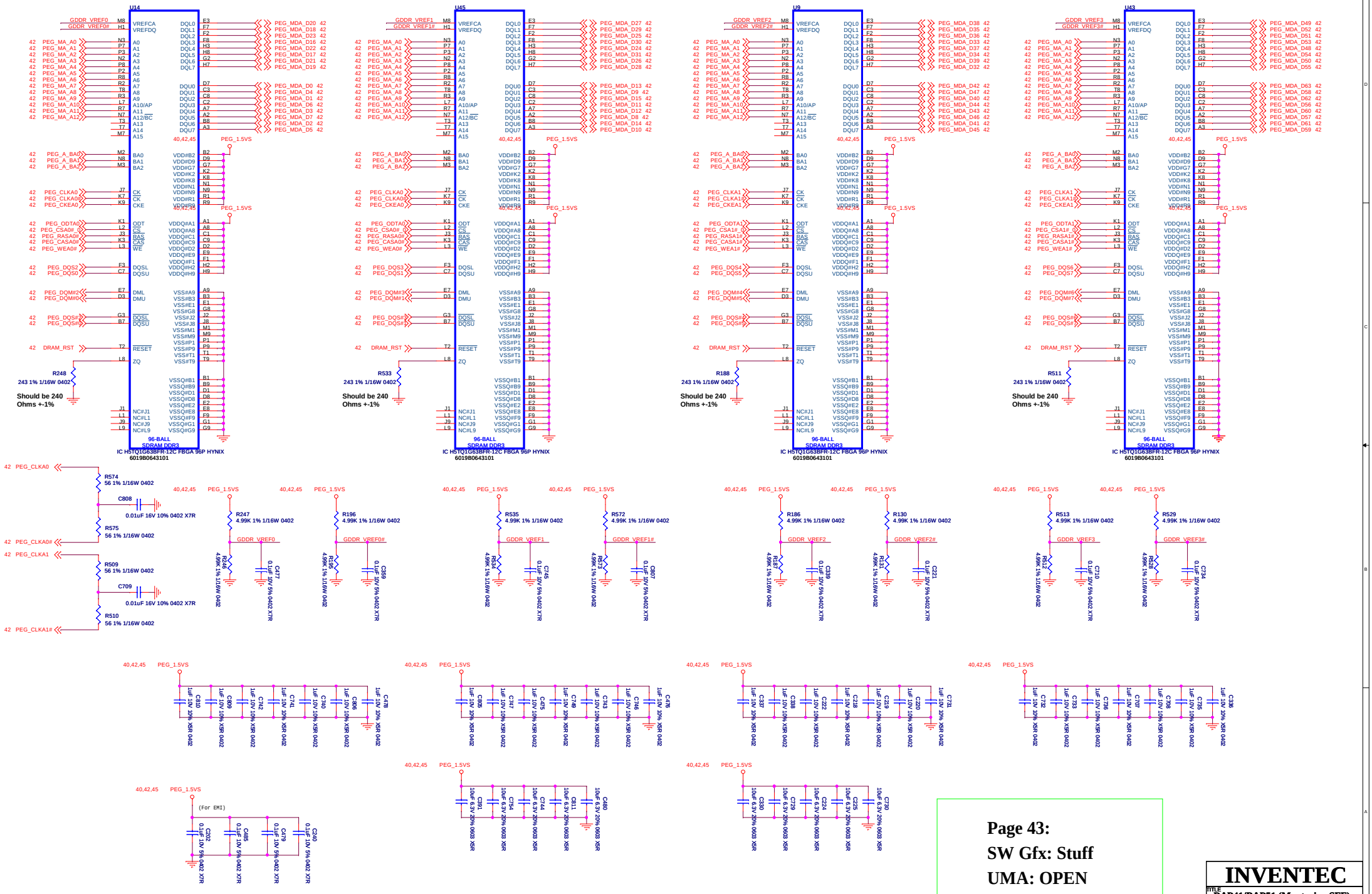




Page 42:
SW Gfx: Stuff
UMA: OPEN

INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) M92			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A2292001-ALG	REV A02
		SHEET 42 of 49	

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009



Page 43:
SW Gfx: Stuff
UMA: OPEN

CHANGE by	Shiun-Chin Chang	DATE	Wednesday, July 01, 2009

INVENTEC

TITLE: **BAP41/BAP51 (Montevina SFF)**
VRAM

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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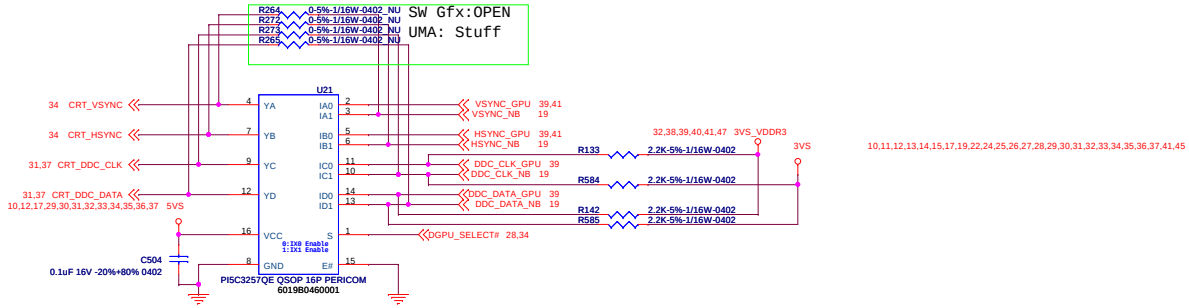
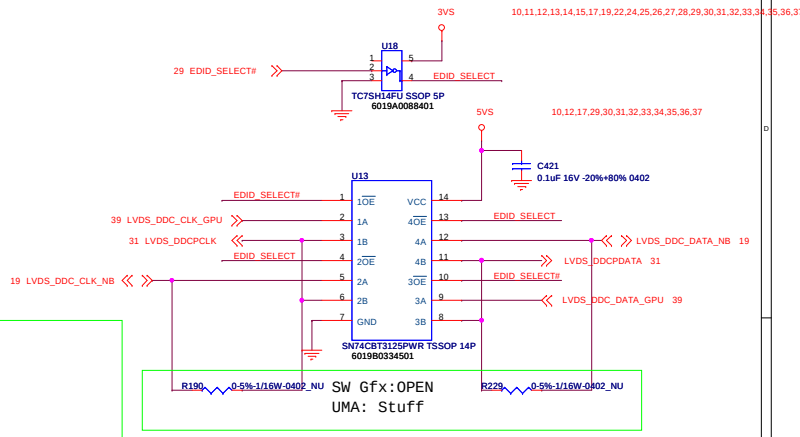
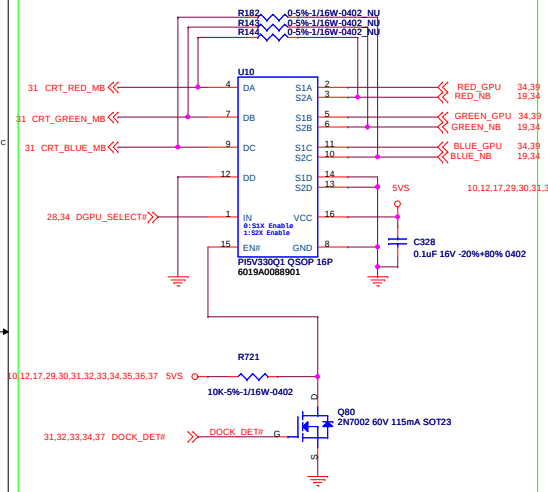
CRT HSYNC/VSYNC/DDC SW



LCD DDC SW



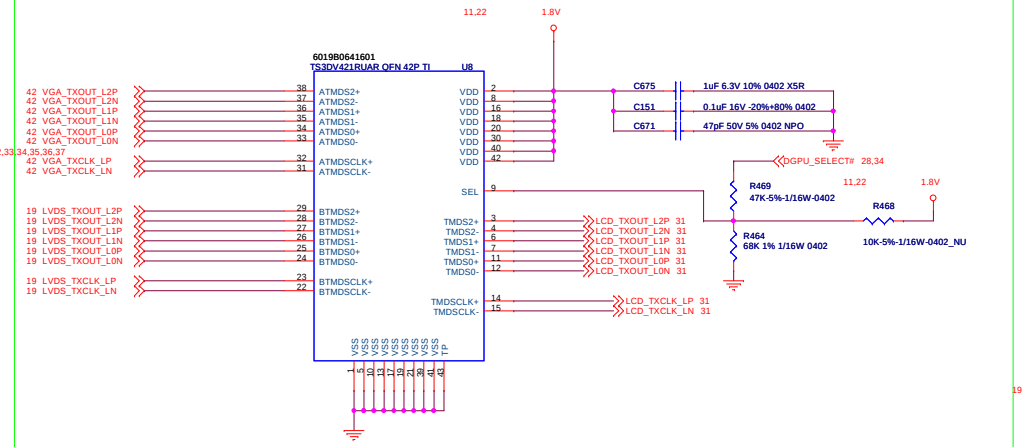
CRT R/G/B SW



Stuff CRT/RGB SW for both SW Gfx and UMA

SW Gfx : Stuff U10,C328,R721,Q80
UMA : Stuff U10,C328,R721,Q80

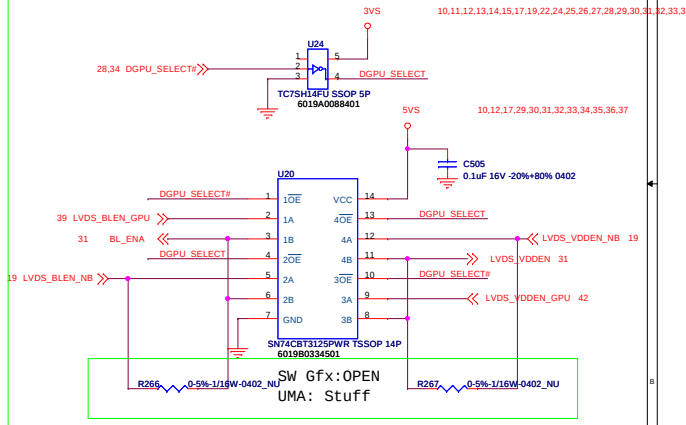
LVDS SW



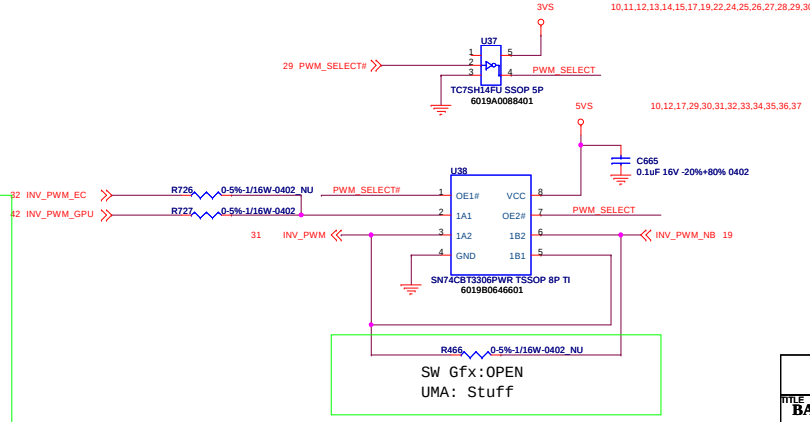
Thermal Pad limitation : Stuff LVDS SW for both SW Gfx and UMA

SW Gfx : Stuff U8,C675,C151,C671,R469,R464, OPEN R468
UMA : Stuff U8,C675,C151,C671,R468, OPEN R469,R464

LVDS BKL and Vcc Enable SW



LCD PWM SW



Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
EDID_SELECT#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

Page 44:
SW Gfx: Stuff
UMA: OPEN

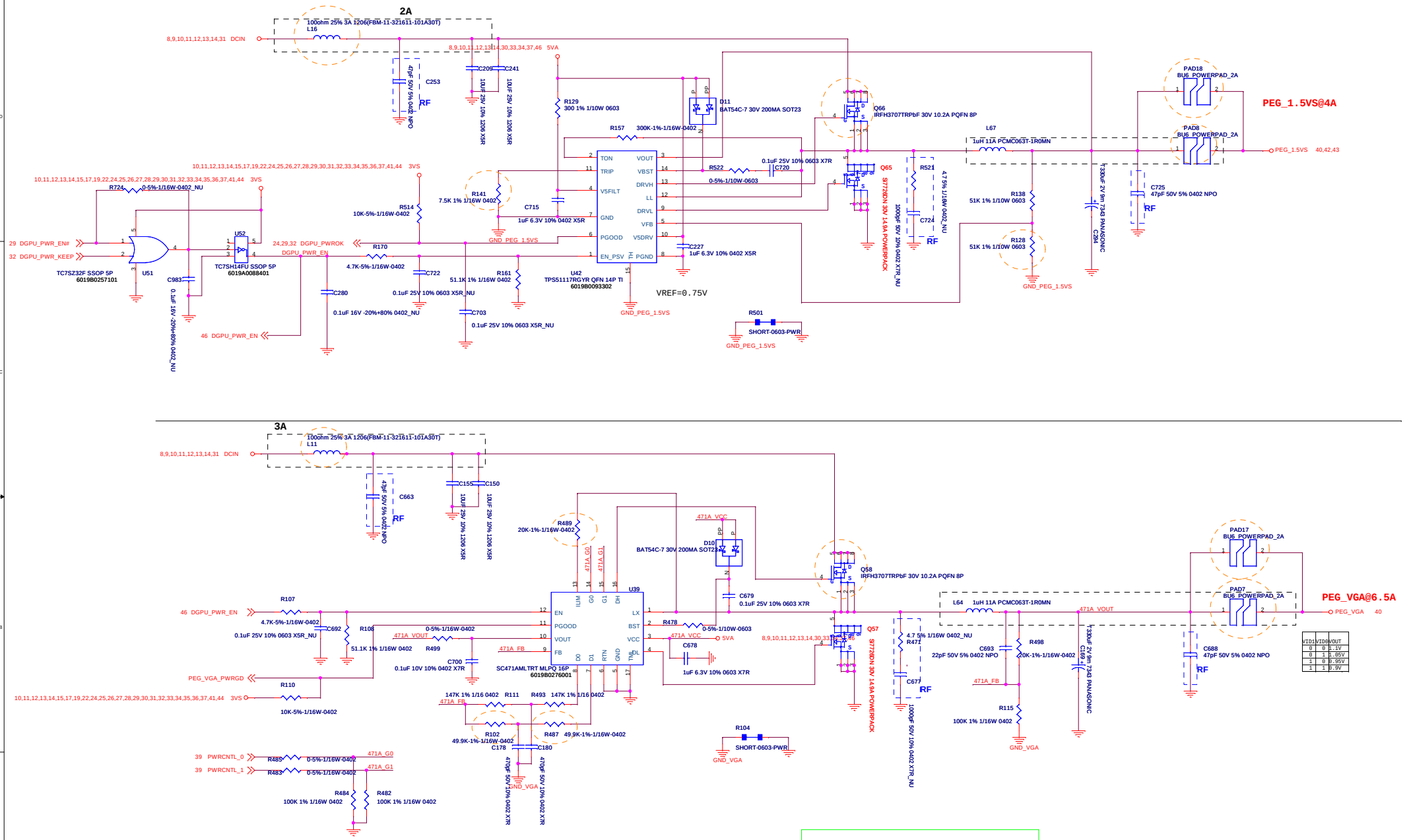
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF) Hybrid switch

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

SHEET 44 of 49

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009



PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

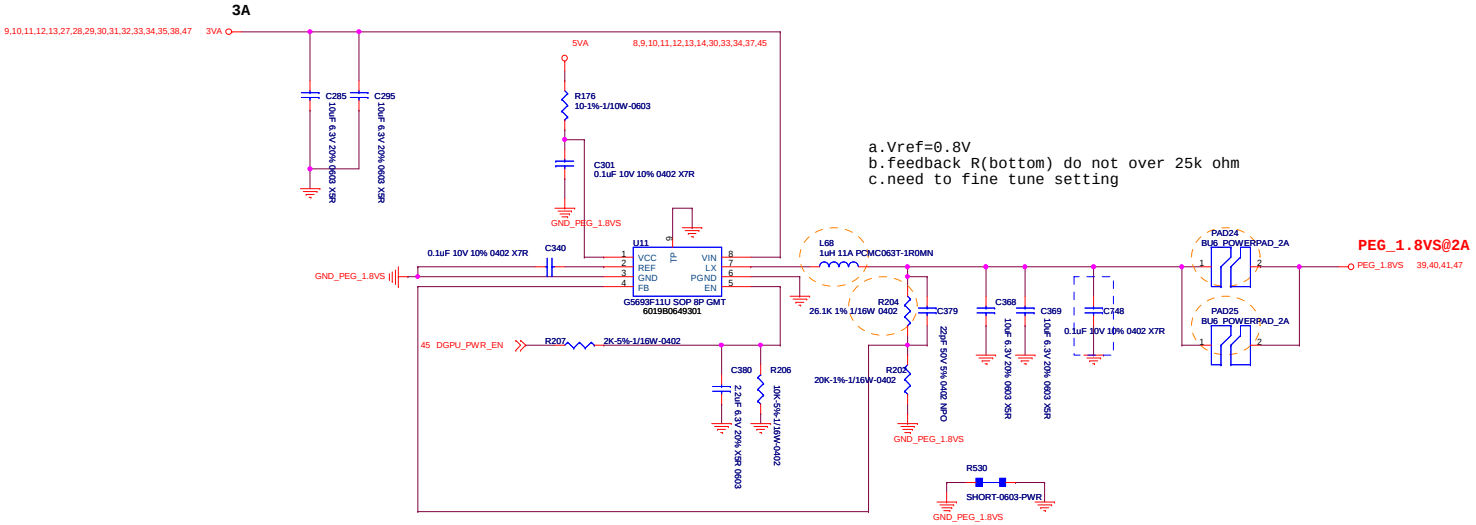
Page 45:

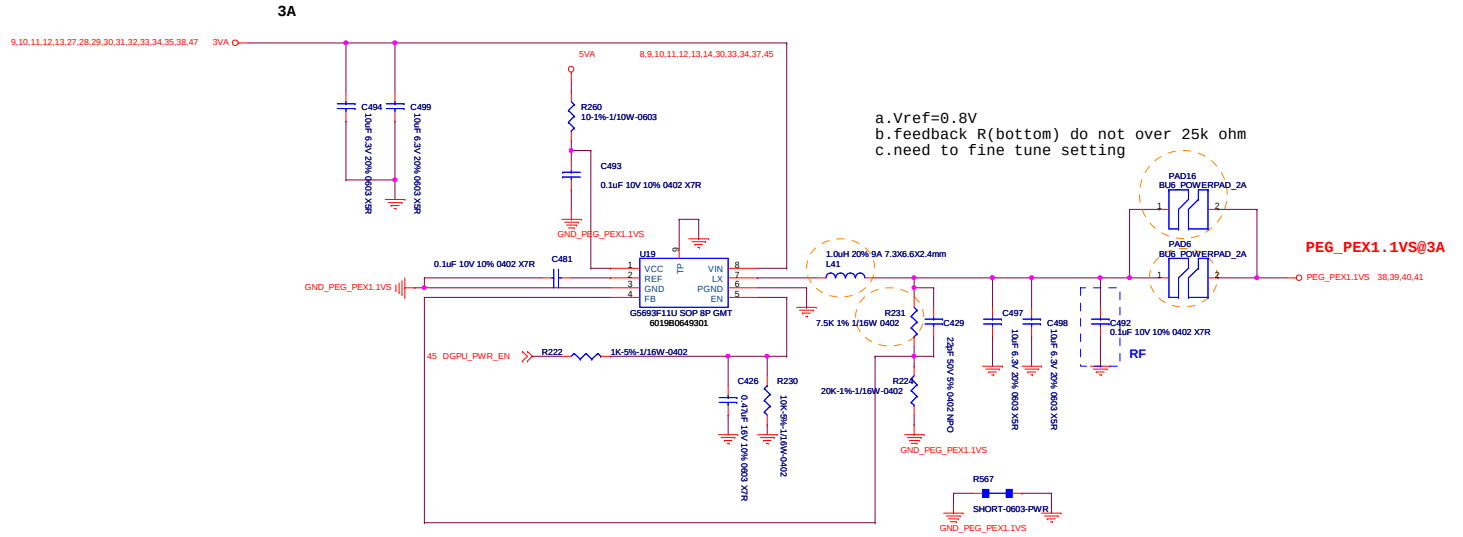
SW Gfx: Stuff

UMA: OPEN

INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) VGA Power			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
		SHEET 45 of 49	

CHANGE by Shiun-Chin Chang DATE Wednesday, July 01, 2009



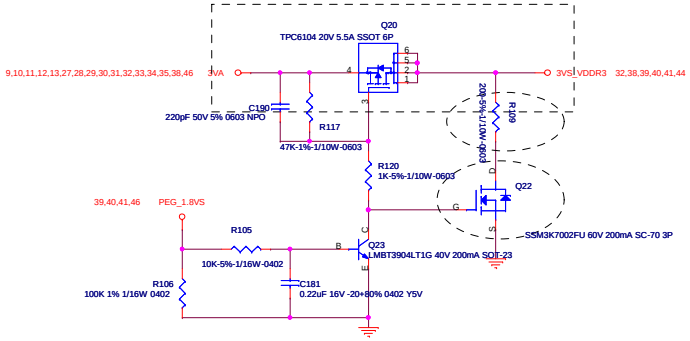


Page 46:

SW Gfx: Stuff

UMA: OPEN

INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) VGA Power			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A229201-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Wednesday, July 01, 2009	SHEET: 46 of 49	



Page 47:

SW Gfx: Stuff

UMA: OPEN

CHANGE by	Shiun-Chin Chang	DATE	Wednesday, July 01, 2009

INVENTEC

TITLE
BAP41/BAP51 (Montevina SFF)
VGA Power

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A229201-ALG	A02

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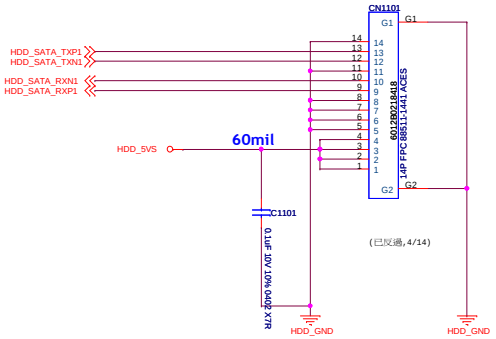
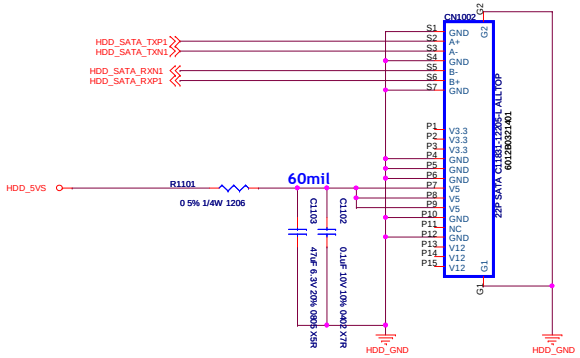
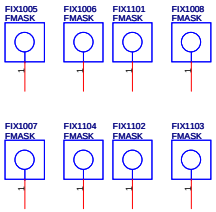
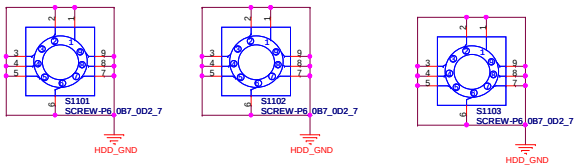
HDD Board CN TO MB



HDD I/F

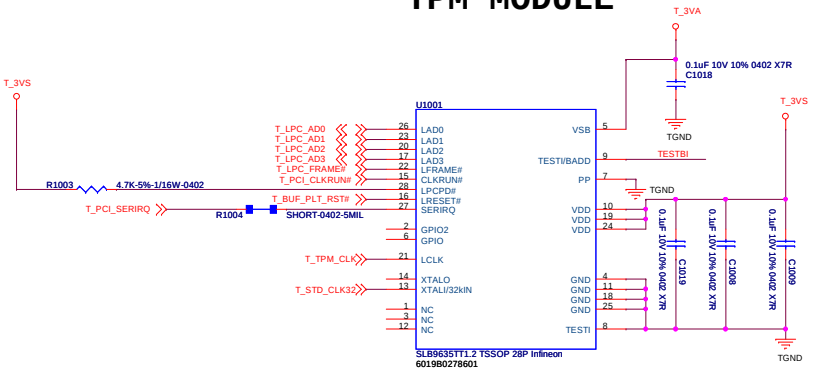




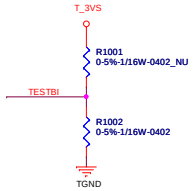


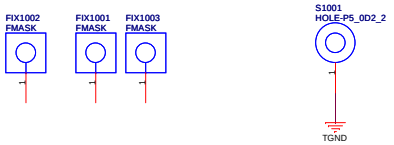
INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) HDD Board			
SIZE Custom	CODE A02	DOC.NUMBER D-CS-1310A229200 1-ALG	REV A02
CHANGE by Shiun-Chin Chang	DATE Monday, June 29, 2009	SHEET 48 of 49	

TPM MODULE

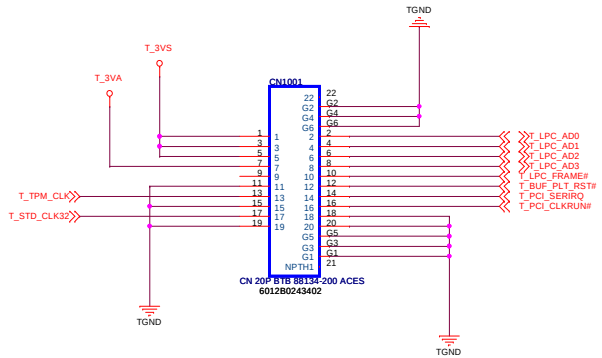


TESTBI	I/O ADDRESS
	CONFIG REGISTER
HIGH	4EH
LOW	2EH





TO MINI-CARD/B



INVENTEC

TITLE
BAP41/BAP51 (Montevina SFF)
TPM Board

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Monday, June 29, 2009 SHEET 49 of 49